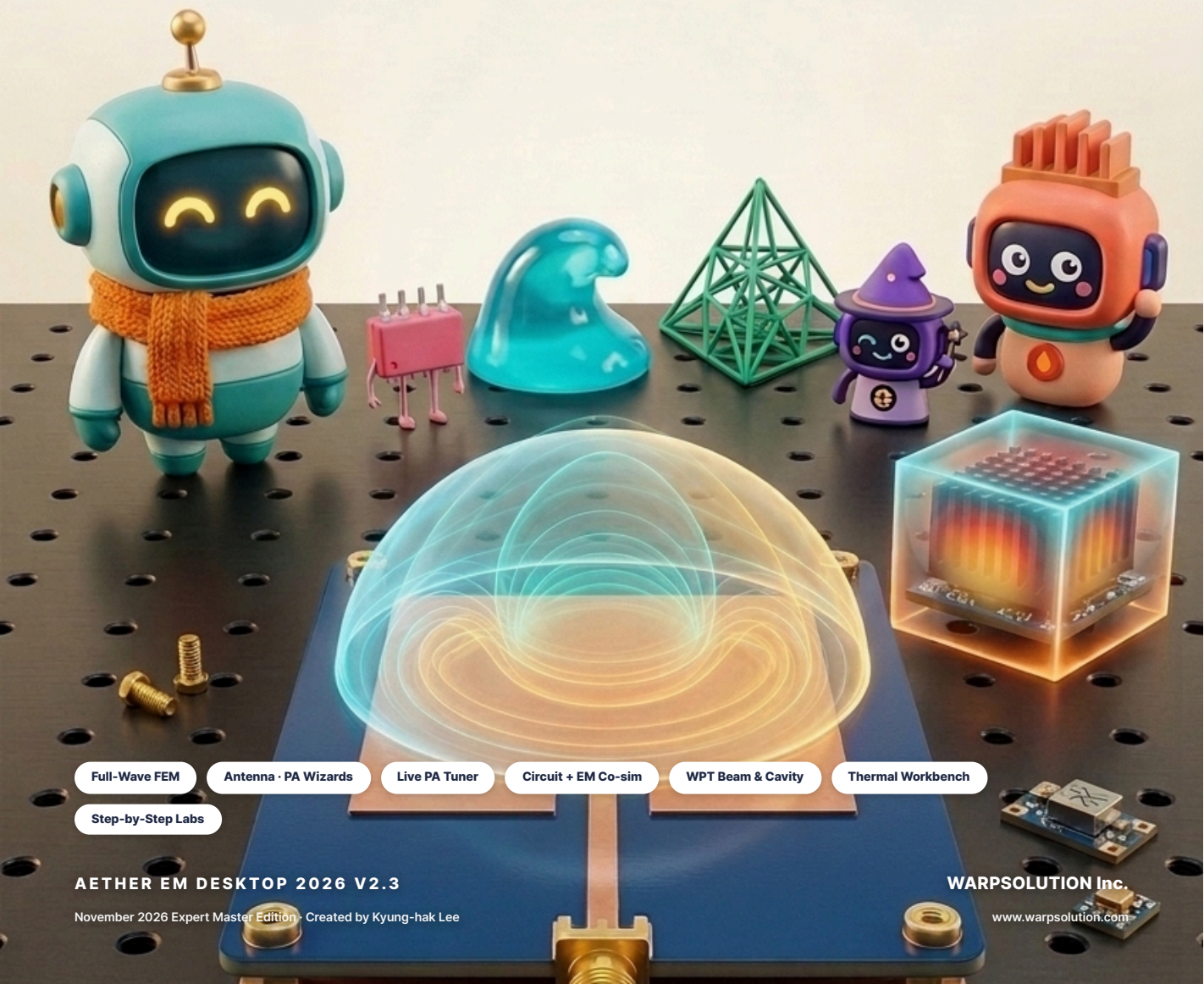
Learn by Pictures

3D EM · Wizards · Thermal Design

Aether EM Desktop 2026 V2.3 Practical Design Guide — from 3D Full-Wave FEM to antenna · PA · WPT auto-synthesis wizards, schematic Co-sim, integrated electro-thermal cooling and full step-by-step labs



Full-Wave FEM | Antenna · PA Wizards | Live PA Tuner | Circuit + EM Co-sim | WPT Beam & Cavity | Thermal Workbench | Step-by-Step Labs

AETHER EM DESKTOP 2026 V2.3

November 2026 Expert Master Edition · Created by Kyung-hak Lee

WARPSOLUTION Inc.

www.warpsolution.com

Aether EM Practical Design Guide — Desktop 2026 V2.3 (Expert Master Edition)

3D electromagnetic analysis learned through pictures and six characters · unrivaled automatic RF synthesis wizards · integrated electro-thermal cooling · hands-on labs & sample encyclopedia

Target software · Aether EM Desktop 2026 V2.3 (Warps 3D Full-Wave FEM & Electro-Thermal Suite)
Reference build · November 2026 edition (previous edition: v1.96 Expert Edition · 9 parts, 42 chapters)
Characters · Aether, Porty, Wavy, Mesh, Wiz, Thermy
Created by · Kyung-hak Lee
Published by · WARPSOLUTION Inc. (www.warpsolution.com)

Every UI screen, six-style rendering viewport, wizard dialog, thermal temperature map and measured-performance chart in this book was captured and verified directly in a real **Aether EM Desktop 2026 V2.3** environment. The figures for antenna auto-tuning, the CGH40010 / CG2H40010 GaN power amplifier (PA) tuner adventure, the black-anodized heat-sink comparison (TH1–TH4), the cavity WPT resonator, the thermal verification benchmarks (Th1–Th8) and the 35+ distributed example files (`.warp`) reproduce actual solver-verified data as is. Always apply every closed-form initial synthesis value to a final production design only after 3D FEM verification and bench calibration.

MEET THE 6 CREW MEMBERS

Six friends guide you through the design lab

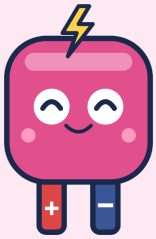
The Desktop 2026 V2.3 edition welcomes two new members: the wizard **Wiz** and the cooling coach **Thermy**! The color and badge of each speech bubble tell you at a glance whether it is a practical tip, a pitfall warning, or a one-of-a-kind weapon you won't find in other tools.



GUIDE · TEAL

Aether

The lab's lead guide robot. Points out the fastest working order and the key shortcuts.



CAUTION · PINK

Porty

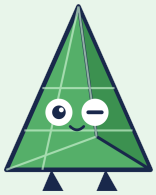
A port fairy with + and – legs. Guards you against easy pitfalls such as polarity, units and reference planes.



THEORY · BLUE

Wavy

An electromagnetic-wave friend. Explains complex Maxwell equations and impedance physics in intuitive picture language.



CHECK · GREEN

Mesh

Guardian of the tetrahedral mesh. Responsible for convergence checks (|ΔS|), energy conservation and catching coarse-mesh illusions.



WIZARD · PURPLE · NEW

Wiz

The auto-synthesis wizard with a Smith-chart medal and a magic wand! Passes on the secret of 1-second formula synthesis (≈) and 3D FEM correction.



THERMAL · ORANGE · NEW

Thermy

The thermal coach wearing a copper heat-sink crown! Handles thermal-bottleneck tracing, TIM · via · anodizing cooling and thermal-runaway prevention.

CREW COMIC **Lab mini-dialogue — why finish in one file the work that used to bounce between four expensive commercial tools?**



Wiz Give me just a few spec numbers, and in 0.2 seconds I'll draw you a patch array and an intrinsic-drain Class-F power amplifier board!

Mesh Wait! A first drawing from formulas (≈) misses the frequency by 1–3 % because of junction fringing. It only becomes a real design after verification with my adaptive FEM mesh and space mapping.





Thermy And however pretty S11 looks, once the GaN chip heats up to 160 °C its efficiency collapses and thermal runaway follows! Let's go straight to thermal analysis too, with no CAD conversion!

Master tutorials

Part 7 missions & Part 8 sample encyclopedia

From a blank `Ctrl` + `N` coordinate entry to the 8-step GaN PA detective mission, with a full walkthrough of 35+ samples.

Menus and ribbons

Results ▸ PA Results

Top menu-bar paths and ribbon button names are shown together, so you never get lost.

The three core badges

NEW V2.3 UPGRADE ONLY IN AETHER

NEW V2.3 new feature,
UPGRADE enhanced feature,
ONLY IN AETHER a unique weapon not found in other commercial EM tools!

ONLY IN AETHER EM · KILLER DIFFERENTIATORS

Not in other commercial EM tools! The 12 unique weapons of Aether EM

In conventional RF design, you wasted days switching among four tools — **3D EM solver ↔ circuit simulator ↔ PCB CAD ↔ thermal analysis (CFD)** — and exporting files between them. See how Aether EM Desktop 2026 V2.3 tears down this barrier inside a single `.warp`.

---

01 · Schematic Co-sim → back-annotation into 3D EM — Ch. 25-35

Tune real Murata chips and diodes with live sliders on a free-wiring SVG schematic, then in one click substitute the ports of the 3D model with real **Lumped RLC boundaries**.

02 · Zero-re-solve 0.1-second real-time PA Tuner — Ch. 24-36

Solve the 4-port board EM just once, and without re-meshing, tune E24 real chips automatically, roll the 400-board factory-yield dice, and balance junction temperature (T_j) per heat sink and thermal runaway in 0.1 second.

03 · Intrinsic-drain Class-F synthesis — Ch. 24-37

Back-calculates **the true die current-source plane** hidden behind the package bondwire (L_{pkg}) and capacitance (C_{ds}), plugs in $2f_0$ short and $3f_0$ open stubs, and cuts the output-section area by 55 %.

04 · Competitive review of external KiCad · ADS schematics — Ch. 23

Reads the matching schematics you built in KiCad (`.kicad_sch`) or ADS/AWR/SPICE as they are, and scores them head-to-head against the wizard's synthesized candidates under identical conditions.

05 · Guaranteed |ΔS|=0 independent thermal workbench — Ch. 27–31

Run thermal analysis instantly on the same 3D model without touching the EM mesh or S-parameters by even one bit! Connects pure **RF Loss → Heat** directly, with reflected and antenna-radiated power subtracted automatically.

06 · Zero mesh blow-ups! Node-split TIM & thin copper — Ch. 28-39

Solves a 50 µm solder layer (node splitting) and a 35 µm copper layer (tangential conduction, 595 → 123.5 °C!) perfectly and mathematically, without adding a single thin 3D mesh layer.

07 · External copper solid → Step to RF Line — Ch. 12-36

With one right-click, promote a dumb copper lump imported from STEP · KiCad · Gerber into a **smart parametric RF line** that knows the substrate beneath it, and attach meanders and stubs right away.

08 · Bench copper-tape measurement back-solver — Ch. 19

Enter the size of the **copper tape** (mm×mm) you cut with a knife and stuck on a stub end while watching the VNA in the lab, and it back-calculates the exact pattern extension for the next PCB Gerber.

09 · Non-destructive GND auto-clearing & Via Fill pH read-out — Ch. 9–10

Move or delete a stub and the carved-out CPWG ground and substrate via holes are restored seamlessly, while the parallel inductance (pH) of the $\lambda_g/10$ via fence is calculated instantly.

10 · Chu physical-limit back-solver & 1-pass space mapping — Ch. 20-34

For an unreasonably tiny antenna request, it presents the theoretical minimum sphere diameter ($2a_{min}$), and with `Solved at` (`retune`) space mapping, finishes in a single re-solve what would take 30 optimizer runs.

11 · Near-field focus WPT · human safety line · cavity charging — Ch. 26

Design Fresnel-number (N_F) focus shifting, retrodirective pilot tracking, the 10 W/m² legal exposure limit and 91.9 %-efficiency 433 MHz metal-chamber resonant charging on a dedicated ribbon.

12 · Standard-free 3-Line de-embedding & six shaders — Ch. 3-18

Strip SMA launch parasitics with just three lines and no expensive TRL calibration kit, and instantly produce patent and paper illustrations with the **webtoon · blueprint · pencil-sketch · X-Ray** shaders.

Reading strategy for this book: Watch for the **ONLY IN AETHER** badge throughout the text! It marks Aether EM's own cheat codes, which break in seconds the bottlenecks other tools make you fight with manual scripts and file conversions.

WHAT'S NEW IN DESKTOP 2026 V2.3

Desktop 2026 V2.3 key upgrades & the 9-part master roadmap

Going beyond a plain 3D EM solver, this is the full map of V2.3, completed with **design automation (Wizards) · circuit / nonlinear integration (Co-sim) · wireless power transfer (WPT) · integrated electro-thermal cooling · a complete hands-on encyclopedia**.

Area · key feature	What is new and why it is powerful	Ch.
Six 3D Looks & Open preview NEW V2.3	**Realistic · 2D Webtoon · Blueprint · Pencil Sketch · X-Ray · Height Colors** real-time shaders, and an Open dialog with **.warp 3D preview**, Korean-initial search and 18 templates	3–4
Bondwire · via · Murata chip NEW V2.3	JEDEC 4-point **Bondwire**, $\lambda_g/10$ auto **Via Fill** (parallel pH calculation), 54 **Murata** real parasitic resonances (SRF) from **.s2p**, bidirectional butterfly stub	9–10
Fast STEP import & RF promotion ONLY IN AETHER	Binary-blob-cached fast STEP/NURBS DXF import, direct **Faces** editing (Push-Pull/Heal), and **Step to RF Line** that turns external copper solids into parametric lines	7, 12
Fast ROM sweep & Bayesian optimization UPGRADE	Projected-ROM (**_ProjectedROM**) fast sweep, parallel workers, and **Optuna Bayesian (TPE)** surrogate optimization that finds the answer with the fewest FEM runs	14–15
Publication-grade AePlot · 3-Line de-embedding NEW V2.3	Double-click modeless **Edit** chart editor (2× PNG/SVG), standard-free **3-Line De-embedding**, passivity-corrected **Vector Fit SPICE**, 60 fps 3D HTML viewer	16–18
Transmission line · matching · filter · coupler ONLY IN AETHER	Harmonic dispersion · **bench copper-tape back-solving (TL Wizard)**, dual Smith · rectifier diode · TLT (**Matching**), parasitic line compensation (**Filter**), single-line fault diagnosis (**RF Circuit**)	19, 22
Two-track antennas & metasurface NEW V2.3	The 22-type array · Pareto · probe feed network **Antenna Wizard** (+ metasurface · FPRA) and the **Antenna Designer** with Chu physical limit, miniaturization and FEM auto-tuning	20–21
Integrated 4-step PA ecosystem ONLY IN AETHER	17-device library + KiCad/ADS competition **PA Wizard** → **Bias Designer** (PDN damping) → **Class-F Auto-Stub** (intrinsic drain · 55 % reduction) → 0.1-second real-time **PA Tuner**	23–24
Free-wiring schematic Co-sim ONLY IN AETHER	Wire EM N-ports, Murata chips and Schottky diodes (200×-accelerated voltage-doubler HB) on an SVG canvas, tune, then back-annotate in one click into **3D EM Lumped RLC**	25
Wireless power · cavity WPT ONLY IN AETHER	Dedicated **wireless power** · beam ribbon and the **WPT Beam** menu. Goubau BCE · Fresnel focus truth · human exposure (10 W/m²) safety limit · 433 MHz **Cavity WPT** resonant charging	26
Integrated electro-thermal cooling · jigs ONLY IN AETHER	Independent **Thermal** workbench (|ΔS|=0) + **RF Loss→Heat** + node-split TIM + via / coin / PCM + **black anodizing (−26 K) · thermal runaway · metal jig**	27–31
Hands-on master tutorials & sample encyclopedia NEW V2.3	**Part 7 (Ch. 32–37)** blank-sheet coordinate entry · arrays · stubs · rectenna · 8-step GaN PA detective mission · jig design + **Part 8 (Ch. 38–39)** 35+ `.warp` & 18 `.py` full-explanation catalog	32–39

Contents

01 Getting Started — Screen · 3D View · Multi-Design Projects — 9

01	Aether EM Desktop 2026 V2.3 at a Glance	10
02	Learning the Screen Layout, 8 Ribbons and 11 Menus	15
03	Working with the 3D View and the Six Rendering Styles (Look)	19
04	Multi-Design Projects, 3D Open Preview, Templates and Examples	22

02 3D Modeling & Practical RF Machining — Shapes · Bondwires · Real Chips · External CAD — 28

05	Basic Shapes · Mouse Drawing · Equation Input	29
06	Precision Selection · Measurement · Parametric Design Variables	32
07	Transform · Array · Boolean · Editing External Solid Faces (Faces)	35
08	Sweeps and Equation Curves: Spirals · Helices · Re-editing	38
09	Practical RF PCB · Bondwires · Smart Vias · Murata Real Chips	41
10	Automatic Copper-Overlap Cleanup (Clear · Push) and DRC Review	47
11	Material Library and Conductor · Dispersive-Medium Modeling	49
12	Fast External CAD (STEP · DXF · KiCad · Gerber) Import and Step to RF Line	50

03 Boundaries · Ports · Fast Solver · Optimization — Getting Accurate Answers Fast — 54

13	Mastering Boundary Conditions · Open Regions (Radiation/PML) · Ports	55
14	Solution Setup · Adaptive Mesh · Fast Frequency Sweep	60
15	Validation · Running · Eigenmode · Optuna Bayesian Optimization	64

04 Reading Simulation Results Easily · Publication-Grade Reports — From One Line of a Graph to the Physical Cause and the Fix — 67

16	How to Read S-Parameters · Smith Charts · Convergence Tables, and AePlot	68
17	Reading 3D E-Field · H-Field · Surface Current and Far-Field Radiation Patterns Easily	73
18	3-Line De-embedding · Vector Fit SPICE · Sharing with the 60 fps 3D Viewer	78

05 Wizards & Automatic Design Encyclopedia — From Spec Entry to Finished Antennas · PAs · Circuits · WPT — 81

19	Wizard Ecosystem Map · Common UX · Transmission Line Wizard	82
20	Antennas in Two Stages: Antenna Wizard · Metasurface · Antenna Designer	86
21	Non-Orthogonal Automatic Routing (Smart Connect) and Array Feed Networks (Auto Feed)	90
22	The Three Manual Circuit-Synthesis Tools: Impedance Matching · Filter · Divider/Coupler	93
23	Power Amplifier (PA) 4-Step Mastery ①: PA Wizard & Bias Designer	96
24	Power Amplifier (PA) 4-Step Mastery ②: Class-F Auto-Stub & Real-Time PA Tuner	99
25	Nonlinear & Free-Wiring Schematic Co-sim (SPICE + EM + Back-Annotation)	103
26	Wireless Power Transfer · Beamforming · Cavity Resonance Workbench (WPT Beam)	106

06 Thermal Workbench & Cooling Design — From Junction Temperature Tj to Black Anodizing and Thermal-Runaway Prevention — 110

27	Intro to the Thermal Workbench: EM Integrity ($\|\Delta S\|=0$) and First Steps in Heat-Transfer Physics	111
28	The Three Heat Sources, Node-Split TIM and the Magic of Thin Copper	116
29	Practical Guide to the Five Cooling Helpers: Thermal Via · Copper Coin · Spreader · PCM · Pulse	119
30	Thermal-Bottleneck Tracing (Heat Path) · Auto-Optimization · Temperature → RF Two-Way Coupling	122
31	[Special Feature] Integrated Electro-Thermal Cooling Design of a GaN PA and the Metal Jig	126

07 Practical Design Tutorial Masterclass — From a Blank Ctrl+N Coordinate Sheet to the 8 GaN PA Missions — 131

32	Tutorial 1 (Beginner) · Dipole & Patch Antenna Drawn by Coordinates from a Blank Sheet (Ctrl+N)	132
33	Tutorial 2 (Lower-Intermediate) · 1×4 Array Auto-Feed · Real-Time Beam Steering · The 80 GHz Phase Incident	135
34	Tutorial 3 (Intermediate) · Shape Playground (rf_shapes_playground) & Mastering 1-Pass Space Mapping	139
35	Tutorial 4 (Upper-Intermediate) · 5.8 GHz WPT Rectenna + 7-Port Rectifier HB & Schematic Back-Annotation	142
36	Tutorial 5 (Expert Missions) · CGH40010 5.8 GHz GaN PA Tuner Adventure	145
37	Tutorial 6 (Flagship R&D) · CG2H40010 −33 % Miniaturization · Parasitic Audit · Metal Jig Design	151

08 **Distributed Sample Files & Script Encyclopedia**
35+ Practical .warp Projects and a Python Automation Catalog 154

38 Catalog of 29 Samples: EM Verification · Antennas · Metasurfaces · Passive Circuits · WPT 155

39 Thermal Benchmarks (Th1–Th8) · High-Power PA Sample Lineage · 18 Python Scripts 158

10 **Revision Supplement** 175

43 Setup Advisor and the New Speed Defaults 177

44 Results to Files: Export in Full 180

45 Reading Current · E · H · Radiation from One Dipole 184

46 Phase-2 Wireless Power: Tracking · Exposure · Pose · Rectifier · Resonator 187

47 AI Agents and Physical AI 190

48 Screen · Project · Data Features 192

49 Modeling Features 198

50 PA · Rectifier · Thermal · Antenna-Wizard Features 202

\+ Field Cheat Sheet: The New Features on One Page 205

11 **Complete Menu · Ribbon Reference** 206

File · Edit · View · Project · Draw · Modeler · Simulation · Results · WPT · Tools · Help · Ribbon 206

09 **Expert Appendix**
Emergency Troubleshooting · Menu Map · Glossary 161

40 Symptom-Based Troubleshooting Guide 162

41 Complete Shortcut List and the Full Desktop 2026 V2.3 Menu Map 167

42 Support-Scope Matrix · Summary of Physical Limits · Key Terminology Glossary 172

PART

01

Getting Started
Screen · 3D View · Multi-Design Projects

Aether EM Desktop 2026 V2.3 is a practical RF design environment built around a Full-Wave FEM electromagnetic solver that solves Maxwell's equations directly in 3D, with automatic synthesis wizards, circuit Co-sim, wireless power and a thermal workbench integrated in a single window. Part 1 covers the big picture of the whole design loop, the 8 ribbons and 11 menus, operating the six real-time rendering viewports, multi-design projects and 3D file preview.



01 Aether EM Desktop 2026 V2.3 at a Glance

02 Learning the Screen Layout, 8 Ribbons and 11 Menus

03 Working with the 3D View and the Six Rendering Styles (Look)

04 Multi-Design Projects, 3D Open Preview, Templates and Examples

01 CHAPTER

Aether EM Desktop 2026 V2.3 at a Glance



The days of merely analyzing a shape you drew are over. First, let's unfold the whole map of Aether EM, which runs from spec input through automatic synthesis, 3D FEM verification and nonlinear circuit coupling, all the way to heat and cooling back-coupling.

You will learn
Full-Wave FEM and the integrated design scope

Try it
The closed-loop five-step workflow

Key concepts
Wavelength · S-parameters · dB · Q and verification accuracy

1.1 What does it solve, and how far can it design?

The heart of Aether EM is a **frequency-domain 3D Full-Wave finite element method (FEM) solver**. It divides the whole analysis space into a tetrahedral mesh and approximates the electric field **E** directly with Nédélec tangential vector basis functions defined along the tetrahedron edges. Because transmission lines are not replaced by simple equivalent circuits, 3D physical effects that circuit simulators miss, such as via parasitic inductance, electromagnetic coupling between adjacent lines, package bondwire radiation and housing cavity resonance, are fully captured in the result.

There are two main electromagnetic analysis modes. **Driven Modal** applies RF power through a Wave Port or Lumped Port to obtain multiport S-parameters, field distributions and far-field radiation patterns. **Eigenmode** needs no external port: it computes the natural resonant frequency f_r, the unloaded quality factor Q_0 and the mode field distribution of the closed structure itself. From Desktop 2026 V2.3 onward, the **automatic synthesis wizard family, harmonic-balance · schematic Co-sim, the WPT beam · cavity-resonance workbench and the solid heat-transfer FEM workbench** are all tightly interlocked with it.

ANTENNA · META

Antenna · array · metasurface

22-type array wizard, single-element Chu-limit · miniaturization designer, reflectarray · FPRA, 3D patterns and beam steering.

PASSIVE RF

Line · filter · divider

Microstrip · CPWG · stripline, parasitic line compensation for 13 filter types, 10 divider · coupler types, real Murata chips (.s2p).

PA · CLASS-F

Integrated PA design

17-type GaN/LDMOS library, PDN bias tee, intrinsic-drain Class-F stub, 0.1-second real-time PA tuner.

CIRCUIT CO-SIM

Nonlinear · schematic coupling

Schottky rectifier harmonic balance, free-wiring SVG schematic editor, Monte Carlo yield, 3D EM back-annotation.

WPT BEAM

Wireless power · cavity charging

Near-field focused beamforming, Goubau convergence efficiency, human-exposure (10 W/m²) safety zone, 433 MHz cavity-resonance charging.

THERMAL FEM

Integrated electro-thermal cooling

Transistor · RF skin / dielectric-loss heat sources, TIM · thermal via · copper coin · PCM, temperature→RF back-coupling and heat-sink optimization.

1.2 The closed-loop five-step workflow

Whether you start by drawing shapes from scratch or begin with a wizard, every Aether EM design is completed by going around the five steps below. The icons on the **Home** ribbon tab follow exactly this order, from left to right.

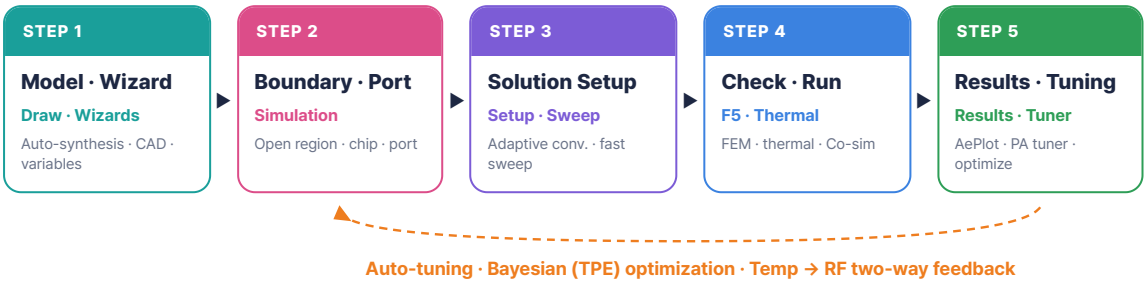


Figure 1-1 The closed-loop design flow of Aether EM Desktop 2026 V2.3. From wizard draft synthesis to 3D FEM, circuit Co-sim and thermal back-coupling, everything goes around inside a single project.

1 Modeling · Wizard	Draw directly with basic shapes and equation variables, or generate a verified parametric starting drawing in 1 second with the antenna, filter or PA wizards.
2 Boundary · Port	Assign the open space (Radiation · PML), conductor-loss boundaries, and the ports that inject and extract the signal (Wave / Lumped / real-chip RLC).
3 Solution Setup	In Solution Setup, set the adaptive-mesh reference frequency and the convergence criterion (|ΔS|), then add fast-sweep bands.
4 Check · Run	Pre-check for omissions and conflicts with F5 Validation Check, then run the Full-Wave FEM with F9 Analyze All.
5 Results · Tuning · Heat	Review publication-grade charts (AePlot), 3D fields, the real-time PA tuner, schematic Co-sim and thermal analysis (Tj), and auto-correct variables or stubs.

FIRST 3 MINUTES **Follow along: your first successful simulation, within 3 minutes of launching!**

1. **Launch the program (`START_WINDOWS.cmd`)**
   Double-click `START_WINDOWS.cmd` in the install folder. The local FEM solver engine starts up and the Aether EM Desktop 2026 V2.3 workspace opens automatically.

2. **Open an example with the 3D preview (`Ctrl` + `O`)**
   From the top menu, choose **File ▸ Open Project...** and click `examples/dipole_antenna.warp` once. Rotate the **real-time 3D preview** that appears on the right of the window with the mouse to check the shape, then press **Open**. (To keep the original intact, it's even safer to save a copy under another name in your own work folder with `Ctrl` + `Shift` + `S` !)

3. **Pre-run health check (`F5`) → run the EM analysis (`F9`)**
   Press `F5` (ribbon **Validate**) and check that all 6 items show a green check, then press `F9` (ribbon **Analyze**). In the `Progress` pane at the bottom of the screen, you'll see the tetrahedral mesh being split, and the analysis finishes in about 30 seconds.

4. **Enjoy your first resonance curve and a living current wave!**
   Click ribbon **Results ▸ S-Parameters** and **a resonance curve dipping sharply to −16.9 dB at 2.95 GHz** appears! Next, click **Results ▸ Surface Current** , then check **Instantaneous** in the right panel and click ▶ **Animate**. The RF current standing wave flowing along the antenna's conductor arms ripples vividly right before your eyes!



Wavy's EM principle note

The E-field and surface-current animations in the 3D viewport take the sinusoidal steady-state phasor $\mathrm{Re}\{\mathbf{E}(\mathbf{r})e^{j\phi}\}$ at a specific frequency f_0 and rotate the phase ϕ from 0° to 360°. It is not time-domain pulse propagation (FDTD), so use it to read standing-wave nodes (nulls) and the phase flow of traveling waves!

1.3 Four physical rulers RF designers use every day

1. Wavelength — the basis of every dimension rule

At high frequencies, whether 10 mm is "long or short" is decided by the **wavelength** λ alone. Even the free-space wavelength $\lambda_0 = c/f$ slows down by the effective permittivity ε_{eff} once it sits on a dielectric substrate, and shortens to the guided wavelength $\lambda_g = \lambda_0/\sqrt{\varepsilon_{eff}}$. Half-wave patches, $\lambda_g/4$ impedance transformers, $\lambda_g/10$ via-fence spacing and $\lambda_0/4$ air-box clearance are all measured in wavelengths.

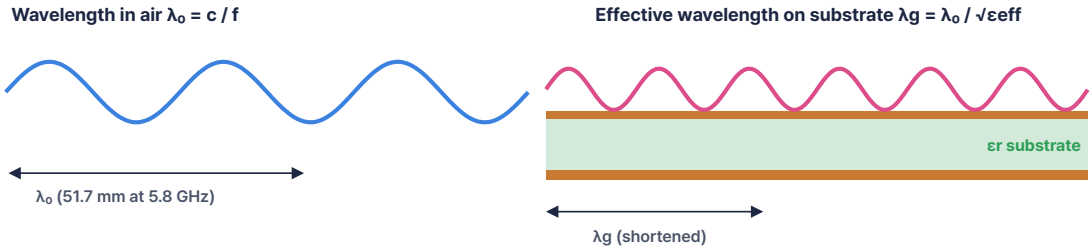


Figure 1-2 The free-space wavelength λ_0 and the effective wavelength λg on a dielectric substrate. Even at the same 5.8 GHz, the wavelength shrinks to about 60 % on an RO4003C substrate.

Typical band	Free space λ_0	Air clearance $\lambda_0/4$	RO4003C $\lambda_g/4$ (approx.)	Representative examples · applications in this book
433 MHz	692.4 mm	173.1 mm	106 mm	Cavity-resonator WPT for robot charging (Ch. 26)
2.45 GHz	122.4 mm	30.6 mm	18.8 mm	Small BLE/Wi-Fi meander · spiral antennas, PA load-pull
5.8 GHz	51.7 mm	12.9 mm	7.9 mm	Patch arrays, WPT beamforming · rectennas, CGH40010 GaN PA (Ch. 36)
10 GHz	30.0 mm	7.5 mm	4.6 mm	WR-90 waveguide, X-band horn, default frequency of a new Setup
77–80 GHz	3.75 mm	0.94 mm	0.58 mm	Automotive radar patch arrays, mmWave bondwire transitions

2. S-parameters · dB · Q — reflection, transmission, and the sharpness of resonance

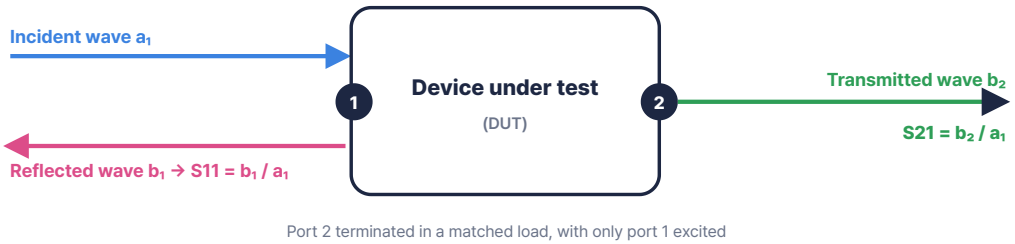


Figure 1-3 Incident waves (a) and reflected · transmitted waves (b) of a 2-port network. They are defined with every unused port terminated reflection-free in the reference impedance Z_0.

S-parameters measure ratios of power waves rather than voltages. If $|S_{11}|_{\text{dB}} = 20\log_{10}|S_{11}|$ is -10 dB or below, at least 90 % of the incident power has been accepted into the structure.

The **quality factor** Q is the ratio of the energy stored per cycle to the power lost ($Q = \omega W / P_{loss} \approx f_0 / \Delta f_{3\text{dB}}$). For filters and cavity resonators, high Q is everything; broadband antennas, on the other hand, need a low radiation Q (Chu limit, Ch. 20) to widen their bandwidth.

$\lvert S_{11}\rvert$ (dB)	VSWR	Reflected power	Accepted power
−3 dB	5.85 : 1	50.0 %	50.0 %
−6 dB	3.01 : 1	25.1 %	74.9 %
−10 dB	1.92 : 1	10.0 %	90.0 %
−15 dB	1.43 : 1	3.2 %	96.8 %
−20 dB	1.22 : 1	1.0 %	99.0 %
−30 dB	1.07 : 1	0.1 %	99.9 %



Porty's port · boundary caution

Don't cheer just because you got $|S_{11}| = -25$ dB! Even when a lossy FR-4 substrate or a damping resistor swallows all the power as heat, the reflection still comes out small. Always check **Radiation Efficiency** for antennas, and the $|S_{21}|$ insertion loss for passive circuits, as well.

1.4 Solver verification accuracy and honest support boundaries

These are Aether EM's verification errors against standard electromagnetic and thermal benchmarks for which exact analytical solutions exist.

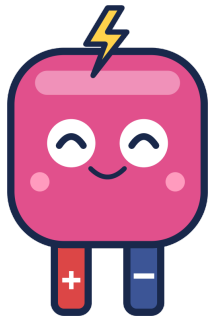
Verification benchmark	Analytical solution	Aether EM V2.3	Relative error
WR-90 waveguide TE_{10} cutoff frequency	6.5571 GHz	6.5600 GHz	0.04 %
Rectangular cavity TE_{101} eigenfrequency (higher-order elements)	9.0076 GHz	9.0078 GHz	0.002 %
Lossy dielectric cavity $Q_d = 1/\tan\delta$	1000.0000	1000.0003	3×10^{-7}
Copper-wall cavity Q_c (Pozar Eq. 6.46)	9182	9178	0.04 %
Half-wave dipole input impedance / max directivity	73 Ω / 2.15 dBi	69 Ω / 2.18 dBi	4 Ω / 0.03 dB
Thermal energy-conservation error $\lvert\Sigma Q_{in} - \Sigma Q_{out}\rvert$ (Th1–Th8)	0 W	$< 10^{-12}$ W	Machine-precision level

Solver boundaries to know before you start

The Full-Wave FEM does not support infinite periodic Floquet unit-cell boundaries, multi-conductor mode separation for differential Driven Terminal, or complex Eigenmode with open radiation boundaries (the metasurface wizard does, however, support synthesis through an equivalent-sheet / guided-wavelength model). The thermal workbench solves **solid conduction + surface convection coefficient h + Stefan–Boltzmann radiation**, and does not include CFD that computes the airflow field itself. For settings outside the supported range, F5 Validation tells you so before the run, with clear messages in Korean and English.

02 CHAPTER

Learning the Screen Layout, 8 Ribbons and 11 Menus



Desktop 2026 V2.3 adds a huge set of wizards and the thermal and wireless-power workbenches, yet it is designed so that the tree and ribbon switch cleanly with the work context. Learn three ways to find the command you want within 2 seconds.

You will learn

The 11 key areas of the workspace

Try it

The 8 ribbon tabs (including Thermal · WPT Beam)

Key concepts

The 11 pull-down menus and automatic hierarchical submenus

2.1 The Aether Desktop 2026 V2.3 workspace at a glance

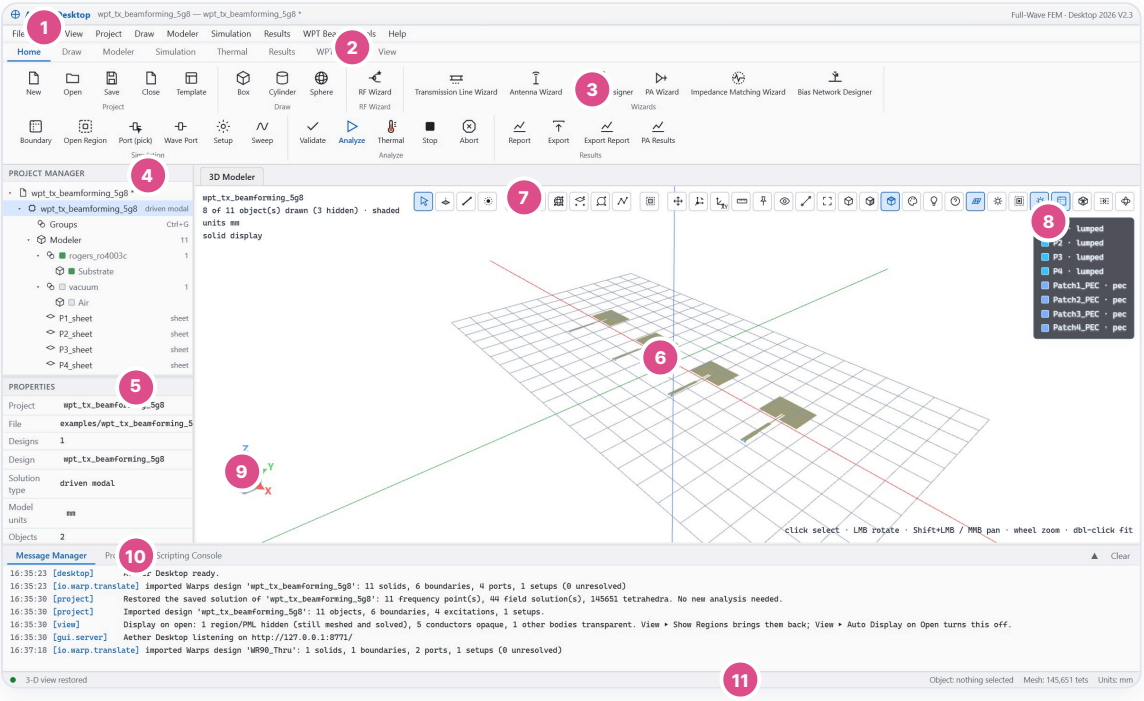


Figure 2-1 The full Desktop 2026 V2.3 screen with the 5.8 GHz 4-element beamforming array (wpt_tx_beamforming_5g8.warp) open. The Full-Wave FEM · Desktop 2026 V2.3 badge appears on the title bar at the upper right.

1. **Menu bar (11)** — every command, from File to WPT Beam, Tools and Help
2. **Ribbon tabs (8)** — Home, Draw, Modeler, Simulation, Thermal, Results, WPT Beam, View
3. **Ribbon icon bar** — the current tab's key tools and the 6 design wizards, arranged by group
4. **Project Manager** — multi-design, solids · sheets by material, coordinate systems, boundary · port · setup · result tree
5. **Properties pane** — instantly edit the values, expressions, color and transparency of the selected object, port or setup
6. **3D modeler viewport** — shape modeling, port picking, rendering of 3D EM fields · temperature fields · radiation patterns
7. **Viewport top toolbar (27)** — object / face / edge / vertex selection, point drawing, measurement, **Look style**, overlay toggles
8. **Boundary · port legend** — assigned ports (lumped / wave) and conductor boundaries (pec) shown by color
9. **View axis triad** — click a disc to switch to an orthographic view; the current tool's mouse hint appears at the lower right
10. **Bottom dock** — Message Manager (history · warnings), Progress (convergence · time remaining), Scripting Console
11. **Status bar** — analysis state, active coordinate system (CS), selected object, tetrahedral mesh count, model units

2.2 8 ribbon tabs: a workbench that follows the design flow UPGRADE

The V2.3 ribbon has grown to 8 tabs. In particular, the **6 core design wizards** sit permanently at the right of the Home tab's top row, so even in an empty project a single button starts antenna, transmission-line, PA, matching or bias synthesis right away.

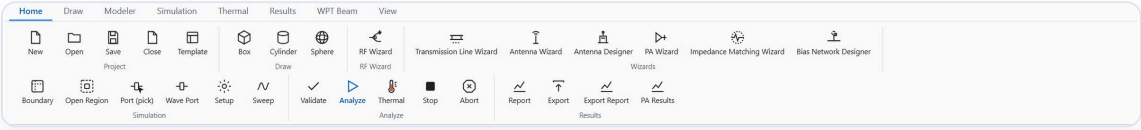


Figure 2-2 The renewed Home ribbon tab. The top row holds Project · Draw · RF Wizard · the 6 Wizards, and the bottom row neatly holds Boundary / Port · Analysis / Thermal · Report / PA Results.

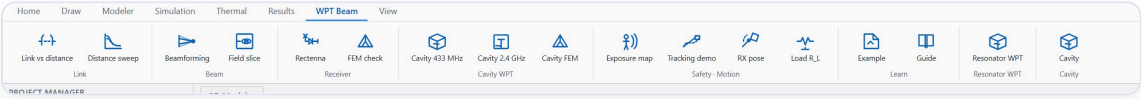


Figure 2-3 The WPT Beam ribbon tab, new in Desktop 2026 V2.3. It guides you through the whole process: link budget, beamforming, rectenna verification, 433 / 2.4 GHz cavity resonators, human exposure and moving-target tracking.

Ribbon tab	Main tool groups
Home	File / templates, basic shapes, **RF Wizard**, **6 Wizards** (TL · Antenna · Designer · PA · Matching · Bias), boundary · port · setup, Validate · Analyze · **Thermal**, Report · **PA Results**
Draw	6 kinds of 3D solids, sheet shapes, **Bondwire**, line / equation curves, CAD import / repair / S-Param PCB, RF Wizard, Smart Connect, Filter Designer, Auto Feed Network · Feed Tune, 6 Wizards
Modeler	Undo / Redo, Boolean · Split · Slice, point-based move / rotate / array, Smart Connect, Sweep, equation curves · coils, **RF machining** (Meander · Stub · Z0 · C/L · Class F · SMD · **SMD @ Point · Via Fill**), **Faces editing**
Simulation	Diagnostics · Controls · Air Region, **Optimize (Bayesian TPE)** · Parameter Study, boundaries · Lumped RLC, Wave / Lumped Port, Setup · Sweep · Mesh, Validate F5 · Analyze All F9

Ribbon tab	Main tool groups
Thermal UPGRADE	Click it and the left tree **switches to the thermal workbench tree** automatically! Thermal settings · materials, Transistor · Heat Source · **RF Loss→Heat**, Face BC · **Contact/TIM** · Thin Copper, via · coin · spreader · PCM · pulse, **Optimize Tj** · **Temp→RF**
Results	S-Parameters · Smith · stability, Port Modes, Eigenmodes, Far Field · antenna summary, 3D E/H/J fields · Cut Plane, **Vector Fit / SPICE**, Export
WPT Beam NEW V2.3	Link budget · distance sweep, beamforming / 3D field slice, rectenna · FEM verification, **cavity resonator (433 MHz / 2.4 GHz / FEM)**, human-exposure map · moving-target tracking · RX pose · rectifier load
View	Fit All · standard views, Shaded / Edges / Wireframe / Solid, **Look (6 shaders)**, grid · Radiation · PML toggles, **Why blank?** diagnosis

2.3 The 11 pull-down menus and two handy rules NEW V2.3

The **11 pull-down menus** at the top hold everything, right down to the advanced tools that don't fit on the ribbon (**Results ▸ 3-Line De-embedding...** , **Results ▸ Co-sim (Circuit + EM)...** and so on). When you read the V2.3 menus, knowing two rules makes things much faster.

- **The top menu bar shows clean English labels** — even when an internal command name carries a Korean explanation, the top pull-down menus keep only the English keywords and render them concisely. For example, the integrated schematic analyzer is *Schematic Co-sim (Circuit + EM)* in right-click menus and window titles, but in the top menu bar it appears as **Results ▸ Co-sim (Circuit + EM)...** or **Tools ▸ Co-sim (Circuit + EM)...** .
- **Three or more related items are grouped automatically into a ▸ hierarchical submenu** — as with **File ▸ Import ▸** , **File ▸ Export ▸** , **Modeler ▸ Faces ▸** , **Modeler ▸ RF ▸** , **Simulation ▸ Assign ▸** and **Results ▸ PA Results ▸** , hover over the item and the submenu unfolds neatly to the side. (The full map is in the Ch. 41 appendix.)

2.4 Modeless dialogs and right-click shortcuts

The wizard windows and the chart editor (`✎ Edit`) of Desktop 2026 V2.3 support a **modeless / translucent-preview structure that you can move by dragging the ⠿ handle at the right of the window title bar**. With a dialog left open, you can change values while watching a real-time preview in the 3D modeler behind it, showing where a stub or via will appear.



A word from Aether

When you've imported an external STEP board, **the 3D viewport right-click menu** is a treasure chest! Right-click a copper trace and choose **RF ▸ Step to RF Line...** , and the plain solid instantly turns into a smart RF line that knows its impedance Z_0 (Ch. 12).

The three bottom docks and shortcut customization

Message Manager records file fingerprint checks, notes on regions hidden at open, and convergence warnings in time order. Get into the habit of always reading the yellow and red lines. **Progress** shows the tetrahedron count, unknowns (DOF), per-pass convergence error and remaining time in real time, and the **Scripting Console** automates every GUI action with Python JSON-RPC commands.

In **Help ▸ Keyboard Shortcuts** (or **Tools**), you can bind any shortcut you like to every menu command and export it as JSON to carry over, as is, to a lab colleague's PC.

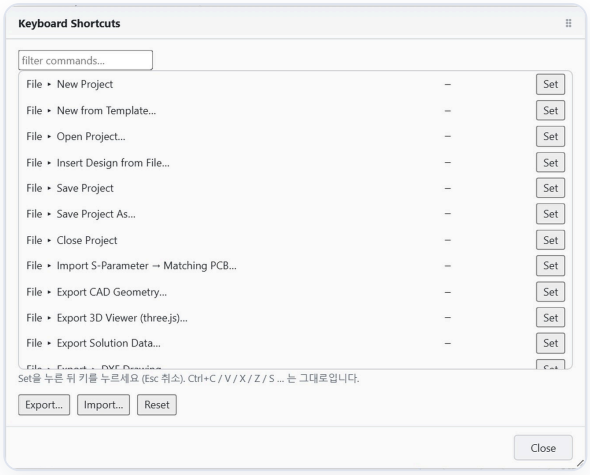


Figure 2-4 The Keyboard Shortcuts settings window. Assign your own shortcuts to the functions you want and back them up or share them as a file.

03 CHAPTER

Working with the 3D View and the Six Rendering Styles (Look)



See through buried vias in a multilayer board with X-Ray, and produce webtoon or blueprint illustrations for patent drawings and presentations with a single click. Master the camera controls you use hundreds of times a day and the six shaders.

You will learn
1:1 Pan · rotation · Alt+click 8-zone view snap

Try it
View ▶ Look: a live gallery of the six renderings

Key concepts
Display on Open and blank-screen diagnosis

3.1 Mouse controls that stick to your fingertips, and 1:1 Pan

In V2.3, the camera Pan recalculates the focal-plane depth in real time so that **the distance the mouse cursor moves matches the point on the drawing exactly, pixel for pixel**. It moves precisely, like pushing a microscope stage, with no sliding or slipping.

Action	Mouse · keyboard	Practical tip
Free 3D rotation	Drag with the left mouse button	Rotates seamlessly past the top and bottom poles, all the way to the ground slot on the back of the board.
1:1 parallel move (Pan)	`Shift` +left drag / wheel-button drag	The grabbed vertex follows the cursor exactly, and the drag continues even when the cursor leaves the window.
Cursor-based zoom	Rotate the mouse wheel	Zooms in smoothly around the feed pin or air gap the cursor is pointing at.
Fit All / Fit Selection	Double-click empty space (`Ctrl` + `D`) / `F`	To fill the view with a single 0402 chip inside a huge air box, select the chip and press Fit Selection.
Instant selection-mode switch	`0` Object · `F` Face · `E` Edge · `V` Vertex	Same as the four leftmost icons on the viewport top toolbar. The starting point for port assignment and face editing.

3.2 To the orthographic view you want in 0.2 s: `Alt` +click 8-zone snap

There are two tricks for aligning the view without opening a menu. First, click a disc of the **X-Y-Z axis triad** at the lower left of the viewport to rotate to face that axis. Second, try **Alt+clicking the empty background of the viewport (or over a transparent air region)**! Click the top, bottom, left or right edge of the screen to snap smoothly to the Top · Bottom · Left · Right orthographic view, or a corner to snap to the isometric view from that direction, in 0.2 s.

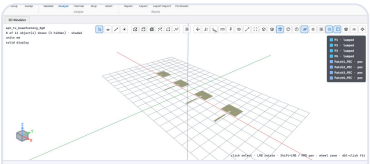


Figure 3-1 Viewport 8-zone Alt+click snap map. Switching to the Top view to check layout alignment takes just 0.2 s.

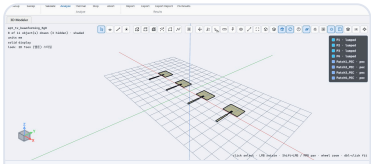
3.3 Six `Look` shaders that transform presentations and multilayer inspection

NEW V2.3

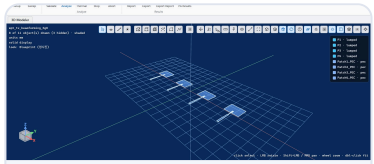
Click the **View ▸ Look ▸** menu, the Look button on the View ribbon, or the palette icon on the viewport top toolbar, and the GLSL post-processing shader changes instantly. These are not mere screenshot filters: **in all six modes, 60 fps rotation, vertex snapping and shape drawing work exactly the same (100 %)!**



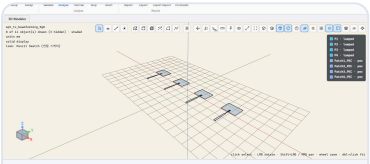
① **Realistic (photoreal)** — The default mode with metallic highlights and shading (follows the light/dark theme automatically).



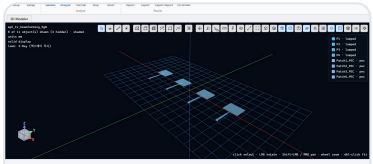
② **2D Toon (webtoon style)** — Crisp cel shading and black ink outlines. Perfect for textbook and presentation-slide illustrations!



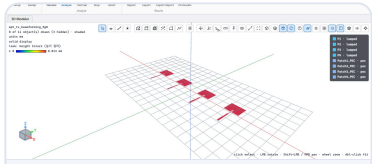
③ **Blueprint** — Precisely highlights white edge lines on a classic engineering-blue drawing.



④ **Pencil Sketch** — Light-and-shade hatching and graphite line art on paper texture, ideal for patent and paper concept diagrams.



⑤ **X-Ray (see-through)** — See through the housing and substrate like translucent glass to inspect inner-layer striplines, thermal vias and copper-coin interference at once!



⑥ **Height Colors** — Maps z-height with the Turbo color map and a color bar at the upper left, so layer steps and bondwire loop heights are clear at a glance.



A word from Aether

When designing a multilayer board, draw patterns in **Realistic** or **2D Toon** as usual, and flip to **X-Ray** only when you check that the inner-layer ground slot and the via barrels really touch. No need to hide and show objects one by one, so your work goes twice as fast!

STEP-BY-STEP **A viewport inspection routine that catches hidden mistakes in a multilayer board in 10 seconds**

1. **Front · isometric view snap**
   `Alt`+click **the top edge** of the empty viewport background to check the planar layout, then `Alt`+click **the upper-right corner** to rotate to the isometric 3D view.

2. **Check inner-layer penetration with X-Ray**
   Choose ribbon **View ▸ Look ▸ X-Ray**. The substrate and pads turn transparent like glass, and you see at once whether the internal via columns and copper coins touch the ground plane without a gap.

3. **Check height steps with Height Colors**
   Switch to **View ▸ Look ▸ Height Colors** and read the color bar (mm) at the upper left; a bondwire apex height or a layer-thickness input mistake (e.g. typing `35mm` instead of `35um`!) shows up immediately in color.

3.4 The Display on Open policy (`Display on Open`) and blank-screen diagnosis

A 3D EM model is wrapped in a large air box (Air Region) and an absorbing layer (PML) outside the antenna or PCB, so if every object is drawn as is, the circuit that matters is hidden inside a white box. When Aether EM opens a file, it analyzes each object's material, boundary and containment relations, and smartly **hides the air region and PML automatically, shows conductors in sharp opaque, and shows the housing and substrate in suitable translucency**.

The most important principle is that **"it only hides the display; the analysis uses it 100 % unchanged."** Whether you hide or show the air box, the mesh and S-parameters are identical down to the last bit. The per-project Display on Open rules can be fine-tuned in **View ▸ Display on Open...**, and to take a quick look at a hidden air/PML box, press the dashed-box icon on the viewport top toolbar.

If you import external CAD and the screen looks empty, don't panic: press **View ▸ Why is the Viewport Blank?...** (ribbon **Blank View?**). It diagnoses the presence, size ratio and transparency of every object and points straight to the cause.

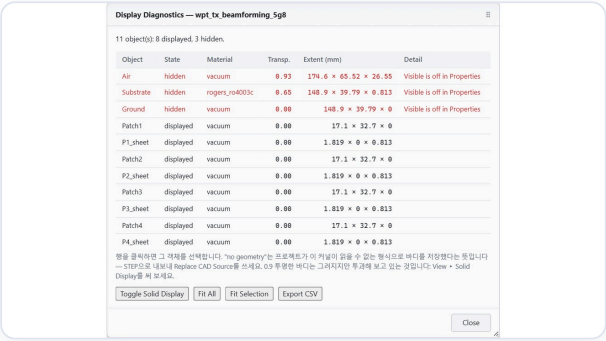
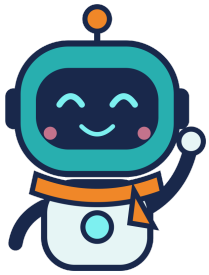


Figure 3-2 The Display Diagnostics window. It tells you clearly, object by object, why a part is too small against the air box or too transparent to see.

04 CHAPTER

Multi-Design Projects, 3D Open Preview, Templates and Examples



Covers smart file management: keeping five variants (initial, optimized and heat-sink cooling versions) side by side in a single `.warp` file for comparison, and rotating the drawing in a 3D preview before you open a file.

You will learn

Managing and merging multiple designs in a single .warp

Try it

Real-time 3D preview in the Open dialog and the .wres fingerprint

Key concepts

18 built-in templates and the full V2.3 example map

4.1 Multi-Design Project Manager: several designs in one file UPGRADE

In real design work, you often need to build a miniaturized patch next to the original to compare them, or manage four cooling variants of the same PA board that differ only in their heat-dissipation structure (no heat sink · natural convection · forced air · black anodizing). **A single Aether EM `.warp` project file can hold any number of designs (Driven Modal / Eigenmode).**

- **Project ▶ Insert Driven Modal / Eigenmode Design** — add a new, empty design
- **Project ▶ Duplicate Active Design** — duplicate the whole current design to create a safe experimental version
- **Project ▶ Insert Design from File (.warp)...** — neatly merge the designs in another `.warp` file into the current project NEW V2.3

Analysis and reports are always run on the **Active Design shown in bold** in the tree. Double-click another design, or right-click it and choose **Set as Active Design**, to switch instantly.

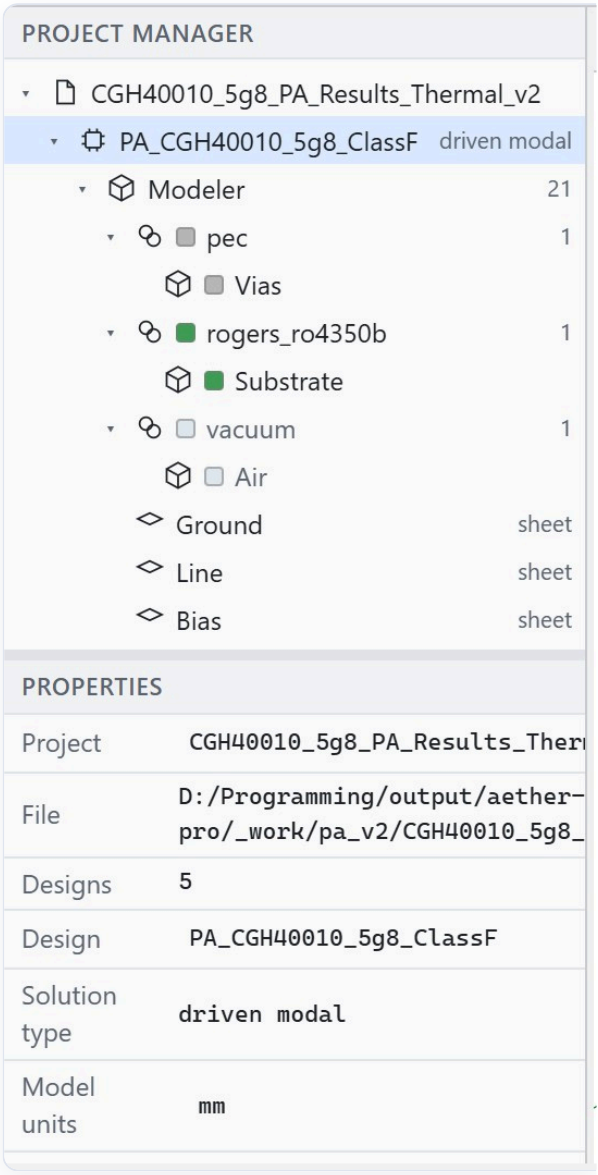


Figure 4-1 An example multi-design project tree (CGH40010_5g8_PA_Results_Thermal_v2.warp). The main PA EM design and four heat-dissipation designs, TH1–TH4, coexist in one file and work together with the PA tuner.

STEP-BY-STEP **Safely testing plan A vs plan B in one file, without touching the original**

1. **Duplicate the whole current design**
   Click **Project ▶ Duplicate Active Design** in the top menu, and a twin design with identical shapes, materials, ports and Setup is added to the left tree immediately.

2. **Give it a clear name, then edit**
   Right-click the new design and name it with `Rename Design…` (e.g. `Ant_Mini_Tuned`), double-click to activate it (bold), then change dimensions with peace of mind and run `F9`.

3. **Compare results back and forth with a double-click**
   Double-click the original and the modified design in the tree in turn, and you can compare the drawings and graphs of the two designs in 0.1 seconds, without opening any file again.

4.2 A real-time 3D preview of `.warp` files you can rotate before opening NEW V2.3

No more opening dozens of version files (`v1`, `v2_stub`, `v3_jig`…) one by one to find the drawing you're after! Open the **Open Project** window with `Ctrl`+`O` and click a `.warp` file in the file list. **The preview pane on the right instantly shows a lightweight 3D drawing you can rotate and zoom with the mouse**, along with the solid / sheet counts, file size, and the number of designs and units it contains.

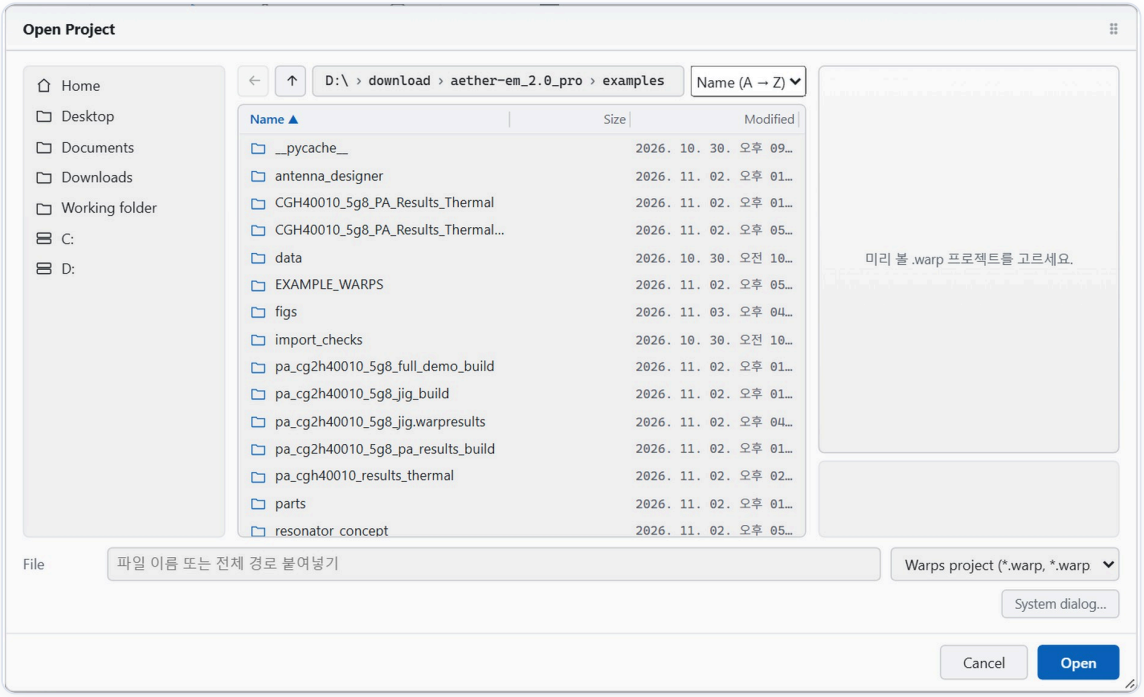


Figure 4-2 The renewed Open Project dialog. Without touching your current working session at all, it shows a safe 3D shape preview and metadata within 1.5 seconds at most, and its file search box also supports Korean initial-consonant search.

4.3 `.warp` and `.warp.wres` — result integrity protected by a SHA-256 fingerprint

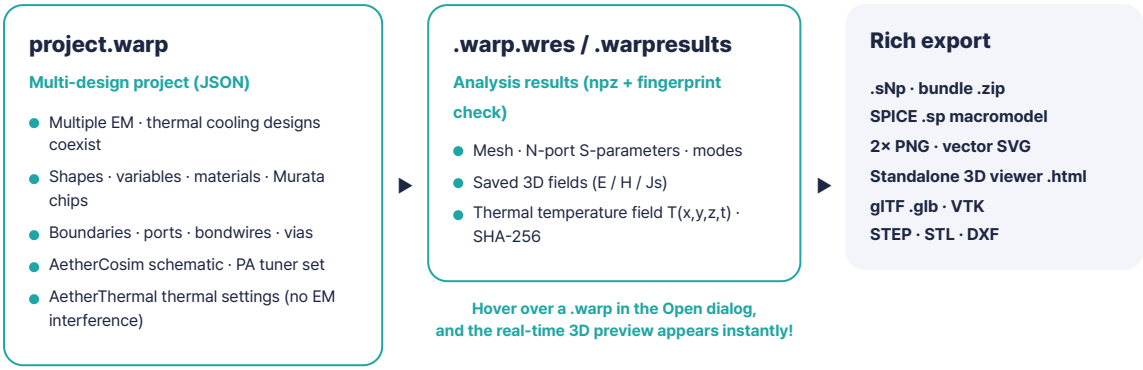


Figure 4-3 The two-part structure of the lightweight JSON design source (.warp) and the large numeric-result sidecar (.warp.wres).

`.warp` is an easy-to-read JSON project file that holds the shapes, parametric variables, materials, ports, thermal settings, schematic Co-sim wiring and even the PA tuner state (external STEP shapes are also stored inside, compressed). `.warp.wres`, on the other hand, holds meshes of hundreds of thousands of tetrahedra and per-frequency 3D electric-field vectors, and is a binary result file created next to it when you save.

When saving results, Aether EM stamps a **SHA-256 cryptographic hash fingerprint** of the `.warp` design state into the `.wres`. If you changed a drawing dimension by even 0.1 mm and saved, it automatically blocks loading the old `.wres`, to prevent the serious mistake of mixing old results with a new drawing, and tells you so honestly in the Message Manager.

4.4 18 starter templates you can analyze with F9 in 1 second UPGRADE

When you're stuck in front of a blank screen, open **File ▸ New from Template...** . V2.3 offers **18 precise starter templates** by category, with substrate, conductors, boundaries, ports, Setup and Sweep 100 % complete.

- **Transmission lines · passives (6)** — 50 Ω microstrip, CPWG, via transition, stepped-impedance LPF, 2-way Wilkinson divider, 90° branch-line coupler
- **Waveguides · resonators (3)** — WR-90 waveguide, inductive-iris bandpass filter, cylindrical cavity resonator (Eigenmode)
- **Antennas · radar (6)** — 2.45 GHz patch, coax-fed patch, 77 GHz automotive radar patch, $\lambda/4$ monopole, X-band pyramidal horn, 2-element fed array
- **WPT · shielding · differential lines (3)** — self-resonant coil pair, slotted metal shield enclosure, 100 Ω differential microstrip pair

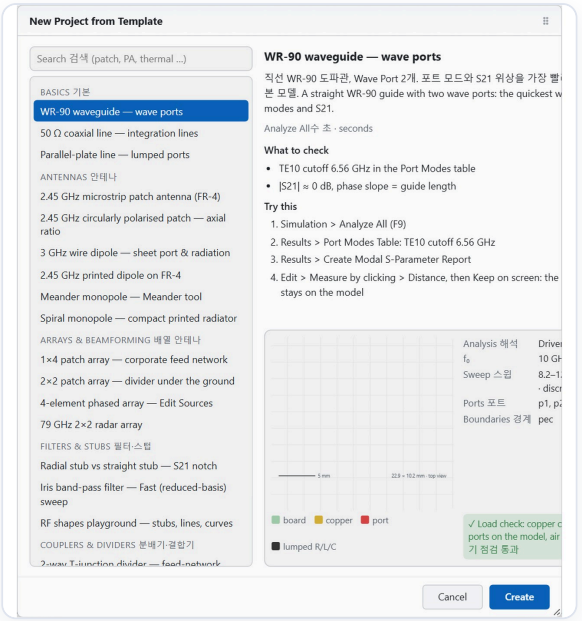


Figure 4-4 The New Project from Template dialog. Choose the structure you want, and a complete model, ready to analyze, opens.

4.5 A map of the bundled example projects, ready for practice

The `examples/` directory in the install folder contains field-verified projects tied directly to each chapter of this book. To protect the originals, always copy them to your work folder before opening them for practice.

Example file (`examples/`)	Key learning topic · related chapters
wr90_waveguide · coax_line · parallel_plate_lumped	Wave Port mode impedance, cutoff frequency, Lumped Port & RLC basics (Ch. 13)
dipole_antenna · patch_antenna · patch_array_1×4_5g8	Dipole · patch far-field efficiency, 1×4 array phased feeding and beam steering (Ch. 32–33)
patch_array_2×2_80g · metasurface_amc_dipole_5g8	80 GHz radar array phase correction, ultra-thin (λ/17) AMC metasurface dipole (Ch. 20, 33, 38)
tee / gysel_divider · radial_stub_notch_5g8	High-power Gysel / T power dividers, wideband radial-stub band-stop comparison (Ch. 34, 38)
slab_matching_parametric · rf_shapes_playground	Bayesian optimization, real-time R·L·C and 1-pass Solved-at space mapping (Ch. 15, 34)

Example file (`examples/`)	Key learning topic · related chapters
wpt_tx_beamforming_5g8 · wpt_wifi_coupling_5g8	5.8 GHz near-field focused beamforming and Wi-Fi channel 165 coexistence scenario (Ch. 26, 38)
wpt_rx_rectenna_5g8 · NT9001 rectifier schematic	Rectenna EM analysis + Schottky-diode HB and schematic back-annotation to 3D (Ch. 25, 35)
CGH40010_5g8_PA_Results_Thermal_v2 NEW V2.3	8-step GaN PA detective mission, real-time PA tuner, TH1–TH4 anodized cooling (Ch. 24, 31, 36)
pa_cg2h40010_5g8_full_demo · pa_cg2h40010_5g8_jig NEW V2.3	Full demo of −33 % miniaturization · package-parasitic audit, and cut-out metal heat-sink jig (Ch. 31, 37, 39)
thermal/Th1_EM_loss_coupling ~ Th8_auto_optimize UPGRADE	8 cases: RF-loss heat source · 220 W coin · thin copper · thermal vias · substrate sweep · PCM · Temp→RF · auto-optimization (Ch. 27–30, 39)

PART

02

3D Modeling & Practical RF Machining Shapes · Bondwires · Real Chips · External CAD

Analysis results are only as accurate as the physics your model captures. In Part 2 you'll learn everything from basic shapes and equation variables, Boolean operations, sweeps and direct face editing to the practical techniques greatly strengthened in Desktop 2026 V2.3: JEDEC bondwires, $\lambda_g/10$ automatic via fill, parasitic resonance from real Murata chips (.s2p), butterfly stubs, and promoting an external STEP board into smart RF lines.



05 Basic Shapes · Mouse Drawing · Equation Input

06 Precision Selection · Measurement · Parametric Design Variables

07 Transform · Array · Boolean · Editing External Solid Faces (Faces)

08 Sweeps and Equation Curves: Spirals · Helices · Re-editing

09 Practical RF PCB · Bondwires · Smart Vias · Murata Real Chips

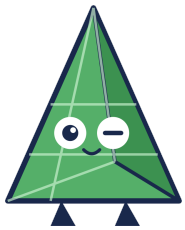
10 Automatic Copper-Overlap Cleanup (Clear · Push) and DRC Review

11 Material Library and Conductor · Dispersive-Medium Modeling

12 Fast External CAD (STEP · DXF · KiCad · Gerber) Import and Step to RF Line

05 CHAPTER

Basic Shapes · Mouse Drawing · Equation Input



Every 3D model starts from basic shapes such as boxes, cylinders and rectangular sheets. This chapter covers how to enter exact numbers, how to sketch with nothing but mouse clicks, and the variable expressions that work in every input field.

You will learn
8 basic solid and sheet shapes

Try it
Point-click drawing and automatic snapping

Key concepts
Unit and expression consistency rules

5.1 Basic Solid and Sheet shapes

The **Draw** menu and ribbon provide **solid shapes** with volume (for substrates, metal enclosures, via barrels and coaxial dielectrics) and zero-thickness 2D **sheet shapes** (for microstrip copper, patches and port faces).

Shape	Type	Key parameters	Practical use
Box	Solid	Position, X / Y / Z size	Dielectric substrate, air box, aluminum jig · heat sink
Cylinder	Solid	Center, Radius, Height, Axis	Single via, coaxial inner · outer conductors, coaxial probe feed pin
Cone · Sphere · Torus	Solid	Radii (r1, r2), height, axis	Conical horn antenna, dielectric lens, magnetically coupled loop coil
Rectangle	Sheet	Position, width · length, plane (XY/YZ/ZX)	Patch antenna, microstrip line, Lumped/Wave port sheet
Circle · Polygon · Ring	Sheet	Center, radius (inner · outer), number of sides	Circularly polarized patch, ring hybrid coupler, round pad

5.2 Numeric input in dialogs and automatic material rules

Open **Draw ▶ Box...** and enter the reference point and size together with units. If you type `25mil` or `35um` after a number, the unit selector on the right switches to that unit automatically.

If you create a box whose name starts with `air`, `vacuum`, `region` or `pml`, its material is set to `vacuum` automatically, and a copper sheet you draw is given a conductor boundary immediately, so it works as a conductor with no extra steps.

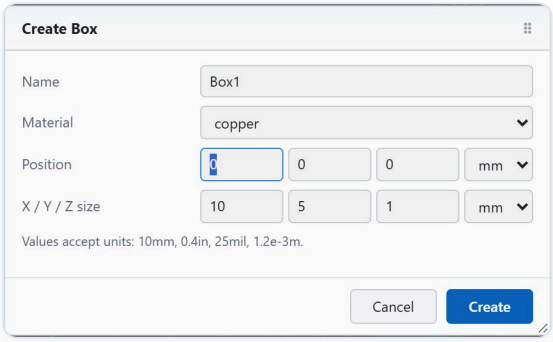


Figure 5-1 The Create Box dialog. Every dimension field accepts numbers, expressions and unit suffixes at the same time.

5.3 Drawing directly with mouse clicks (Draw by Points)

Click a shape icon on the viewport top toolbar and, with no modal window covering the drawing, you sketch boxes, cylinders and rectangles on the 3D view with nothing but mouse clicks. As you move the cursor, it snaps like a magnet to **vertices · edge midpoints · face centers** within 12 pixels (spatial-hash-based 60 fps snapping).

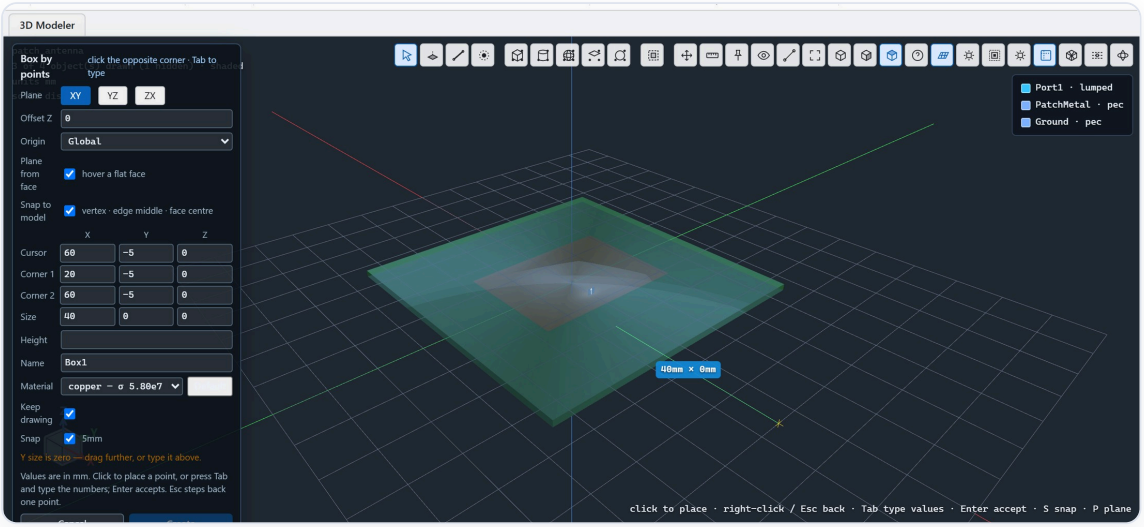


Figure 5-2 Drawing a box by clicking points. Click the first corner and drag diagonally, and a live dimension label and wireframe follow along.

HOW TO **Make a precise box with three clicks**

1. **Check the work plane**
   Switch between the XY · YZ · ZX planes with the `P` key, or hover over the top face of an existing substrate to use that face as the reference plane.

2. **Click the start point → the diagonal point**
   To enter exact values, press `Tab` while dragging, type the numbers into the input fields on the left and press `Enter`.

3. **Set the height**
   Drag the mouse vertically to set the height, and the solid is complete. `Esc` undoes one step at a time.

5.4 An expression calculator that works in every input field

The dimension, frequency and angle fields in Aether EM accept math expressions as they are, such as `PatchL/2 + 0.5mm`, `sqrt(W^2 + H^2)` and `360/8`. The browser preview and the backend CAD kernel share the same parser, so the size you see never differs from the size actually created.

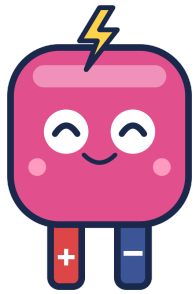


Porty's port · boundary caution

The most common mistake is **leaving out micrometer units**! When the model's default unit is `mm` and you just type `35` into the copper-thickness field, you get **a 3.5 cm-thick copper brick**. Always write thin thicknesses as `35um` or `0.035mm`.

06 CHAPTER

Precision Selection · Measurement · Parametric Design Variables



Applying boundaries, attaching ports and measuring gaps all start from an accurate selection. This chapter sorts out how to pick things hidden behind overlapping objects, the selection rules that depend on drag direction, and the design variables that become the seeds of optimization.

You will learn
The four O · F · E · V selection modes and B -key see-through selection

Try it
Left→right vs right→left drag selection and name filters

Key concepts
Minimum-gap measurement and Design Variables

6.1 Four selection modes and topology-invariant face memory

O · OBJECT
Select object
Material changes, move · duplicate, Boolean operations and other whole-body editing.

F · FACE
Select face
Port · boundary assignment, face Push-Pull editing, local mesh assignment.

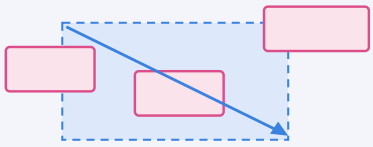
E · EDGE
Select edge
Fillet · chamfer, edge moves, assigning Smart Connect wiring ends.

V · VERTEX
Select vertex
Distance between two points, bondwire pad picking, relative coordinate-system origin.

When an air box or substrate in front hides the patch face behind it, leave the cursor where it is and **press the B key**. The selection steps in turn to the objects and faces behind it along the ray. Also, Aether EM remembers a selected face not by a simple number (ID) but by a **signature of its geometric center, normal vector and area**, so even if you re-mesh later or rebuild after changing a variable, ports and boundaries never jump to the wrong face.

6.2 Area-drag selection and name filters

Drag left → right
Selects anything the rectangle touches



Drag right → left
Selects only objects fully inside

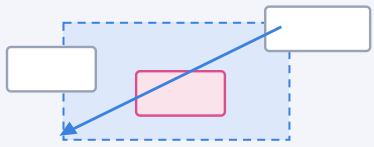


Figure 6-1 Rules for Ctrl+drag rectangle selection. Left→right selects anything merely touched (crossing); right→left selects only objects that lie completely inside the rectangle.

When you need to pick out only certain names among hundreds of via barrels or array patches, open **Edit ▶ Select by Area Filter...** . With wildcard patterns (e.g. `*via*`, `Patch_*`), material, and solid / sheet type, you can select just the objects you want in one go, then change their color or hide them.

As soon as you select, the lower left of the viewport shows the bounding size and **the minimum surface gap between two objects**, measured in real time. Press the `M` key (Measure) to save a precise measurement table as CSV, or use **Keep Current Measurement** to pin the dimension lines on the screen permanently.

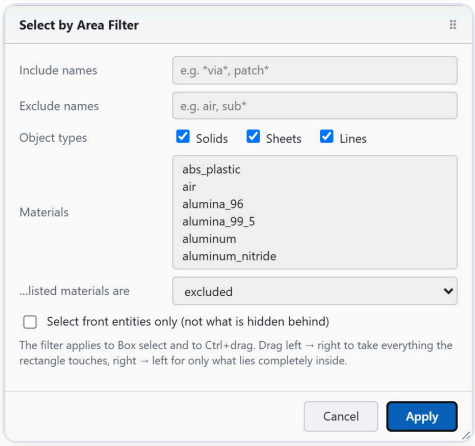


Figure 6-2 Select by Area Filter. It picks out just the group you want, like tweezers, from an assembly of hundreds of parts.

6.3 Design variables (`Design Variables`): the key to studies and Bayesian optimization

Register variables and dependent expressions such as `PatchL = 16.2mm` and `Inset = PatchL * 0.28` in **Project ▶ Design Variables...** (or **Tools**). Then, when you change a single variable value and press **Apply and rebuild**, every related shape, Boolean and port position is regenerated at once.

A built-in unit-dimension checker rules out the mistake of putting a frequency variable into a length field, and the variables you register here become, as they are, the tuning knobs for the **Ch. 15 Parameter Study**, **Optuna Bayesian optimization** and **Ch. 30 thermal Tj auto-optimization**.

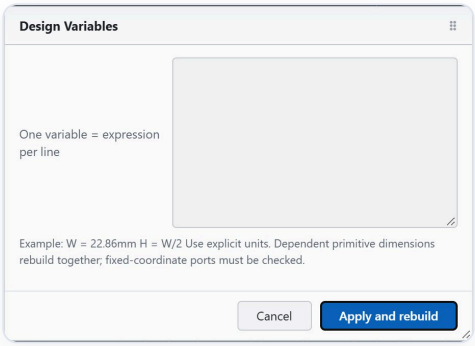


Figure 6-3 The Design Variables editor. It supports expression references and unit checking.

Type	Supported syntax · examples	Practical tips
Length · angle units	`mm, cm, m, um, mil, in, deg, rad`	`20mil` (=0.508 mm) and `35um` (=1 oz copper) are converted automatically when mixed
Frequency · electrical units	`Hz, kHz, MHz, GHz, THz, ohm, pF, nH`	Unit suffixes are recognized instantly in every sweep, port and RLC input field
Built-in math functions	`sin, cos, tan, sqrt, log10, exp, pi`	Enter an initial wavelength value directly as an expression, like `c0/(4*5.8e9*sqrt(2.75))` !

HOW TO **Register your first design variable (PatchL) and rebuild the dependent dimensions in one go**

1. **Open the variable window**
   Open **Project ▶ Design Variables...** from the top menu and press the **+ Add** button.

2. **Register independent and dependent variables**
   Enter `PatchL` as the name and `16.2mm` as the value. Add one more row with the name `Inset` and the expression `PatchL * 0.28` as its value, and the automatically computed `4.536 mm` and a length-dimension pass mark appear on the right.

3. **Link it to the shape's dimensions**
   Click the patch sheet in the tree and, in the length field of Properties at the lower left, type `PatchL` instead of a number.

4. **One-click rebuild**
   From then on, whenever you like, just change `PatchL` to `15.8mm` in the variable window and press **Apply and rebuild**, and the patch, inset notch and port sheet are all regenerated at once with the new dimensions!

07 CHAPTER

Transform · Array · Boolean · Editing External Solid Faces (Faces)



When you move a shape, the ports and boundaries attached to its faces move with it. Along with union and subtract Boolean operations, you'll learn the Faces editing tools that directly fix trace widths and holes in external STEP mechanical parts that have no parametric history.

You will learn
Move · rotate · array with ports and boundaries following along

Try it
Unite · Subtract · Split Booleans

Key concepts
Direct Faces editing (Offset · Delete & Heal · Replace w/ Box)

7.1 Smart transforms and array duplication that move the ports along too

With 40-step snapshot Undo (`Ctrl`+`Z`), you can experiment with confidence at any time.

When you move a shape with move · rotate · mirror · scale in **Edit ▶ Arrange ▶**, or with a two-point click move (the cross-arrow on the viewport toolbar), **the Lumped/Wave ports assigned to that conductor face (including integration-line polarity), boundary conditions and even local mesh operations are transformed along with it automatically**.

In linear · circular array duplication (**Edit ▶ Duplicate ▶**), **Total number is the total count, including the original**. To make a 1×4 patch array, draw one original and enter `4` for Total number.

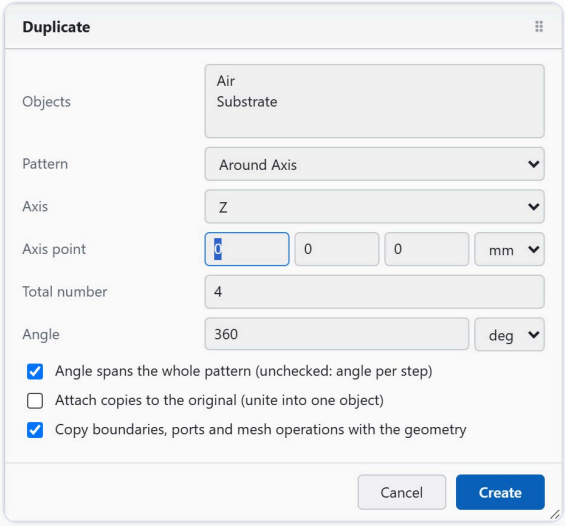


Figure 7-1 Circular array duplication (Around Axis). Useful for building circularly polarized sequential-rotation arrays or cylindrical via rings.

7.2 Boolean operations and plane Split

Command (Modeler ▶ Boolean ▶)	Behavior and practical tips
Unite	Merges several selected conductor sheets or solids into a single continuous object (removing the internal interface faces at the joints).

Command (Modeler ▶ Boolean ▶)	Behavior and practical tips
Subtract...	Cuts the tool object (Tool) out of the target object (Blank). When drilling via holes through several layers, turn on **Keep originals (keep tools)**.
Split by Plane... / Imprint	Cuts a symmetric model in half along the XY · YZ · ZX plane (to use symmetry boundaries), or imprints a contact face so the mesh nodes coincide.

7.3 Even history-free external CAD, at will: direct Faces editing UPGRADE

The STEP housings and antenna brackets you receive from the mechanical team have no design variables. With **Modeler ▶ Faces ▶** in Desktop 2026 V2.3 (or right-click **Faces ▶** after selecting a face with F), you can modify and defeature the shape on the spot, without going back to the original CAD program.

Face · edge command	What it solves
Offset / Push-Pull... NEW V2.3	Pushes or pulls the selected planar or cylindrical face along its normal. Patch-length tuning, cavity-wall moves and via-radius changes take just a second.
Delete & Heal NEW V2.3	Deletes tiny fillets, chamfers and screw-hole faces that eat up tens of thousands of mesh elements, extends the neighboring faces, and automatically heals the result into a clean solid.
Replace with Box NEW V2.3	Simplifies complex connector shells or heat-fin bundles that don't matter to electromagnetic performance into an equivalent outer bounding box, to maximize analysis speed.
Sweep Face · Detach	Extrudes a selected 2D section along its normal into a new 3D solid, or detaches one solid surface as an independent sheet.



Mesh's convergence · accuracy check

A single 0.2 mm logo engraving and one screw thread in an external mechanical STEP can swallow 70 % of the whole tetrahedral mesh! Just tidying away the needless little wrinkles with **Delete & Heal** and **Replace with Box** before the analysis cuts the solve time from 5 minutes to 20 seconds.

HOW TO **Zero mistakes! The Boolean Subtract order, and sealing a hole in an external STEP in 1 second**

1. **Subtract selection order (plate to keep → tool to cut)**
   In the tree or viewport (`O` mode), **first click** the object to be drilled (**Blank**, e.g. the substrate or ground plate), then `Ctrl`+click the pillar to cut out (**Tool**, e.g. a via or coax outer conductor) as the second selection.

2. **Make sure Keep originals is checked!**
   In **Modeler ▶ Boolean ▶ Subtract...**, to stop the via conductor pillar itself from disappearing too, always check **Keep originals (keep tools)** and press **Apply**.

3. **Remove unneeded holes in an external STEP**
   To fill a screw hole in an imported mechanical part, press the `F` key (face select) and click the cylindrical inner wall face of the hole.

4. **Run Delete & Heal**
   Right-click **Faces ▶ Delete & Heal**, and the hole is filled without a trace and automatically restored to a smooth, flat solid!

08 CHAPTER

Sweeps and Equation Curves: Spirals · Helices · Re-editing



From rotationally symmetric horn antennas to Archimedean spirals drawn with parametric equations and 3D helical coils, this chapter covers curve-modeling techniques and the Edit curve feature, which lets you change the equation again after the shape is created.

You will learn
Three Sweeps: axis · vector · path

Try it
Equation Curve · Helix · Spiral

Key concepts
Properties ▶ Edit curve non-destructive re-editing

8.1 Three Sweeps that turn a cross-section into a solid

Modeler ▶ Sweep ▶ moves a planar profile sheet to create a 3D solid. **Around Axis** rotates the section around a given axis to make coaxial tapers, conical horns and dielectric rings; **Along Vector** extrudes it in an oblique vector direction; and **Along Path** sweeps the section, kept perpendicular, along a polyline or equation curve.



Figure 8-1 The Sweep Around Axis dialog. Specify the rotation axis and angle (360° gives a closed solid of revolution).

8.2 Equation curves (`Equation Curve`) and the Helix · Spiral presets

Draw ▶ Equation-Based Curve... and **Draw ▶ Helix... / Spiral...** generate precise curves from the equations $x(_t)$, $y(_t)$, $z(_t)$ of the parameter `_t`. Here, the choice of **Make (cross-section type)** is critically important.

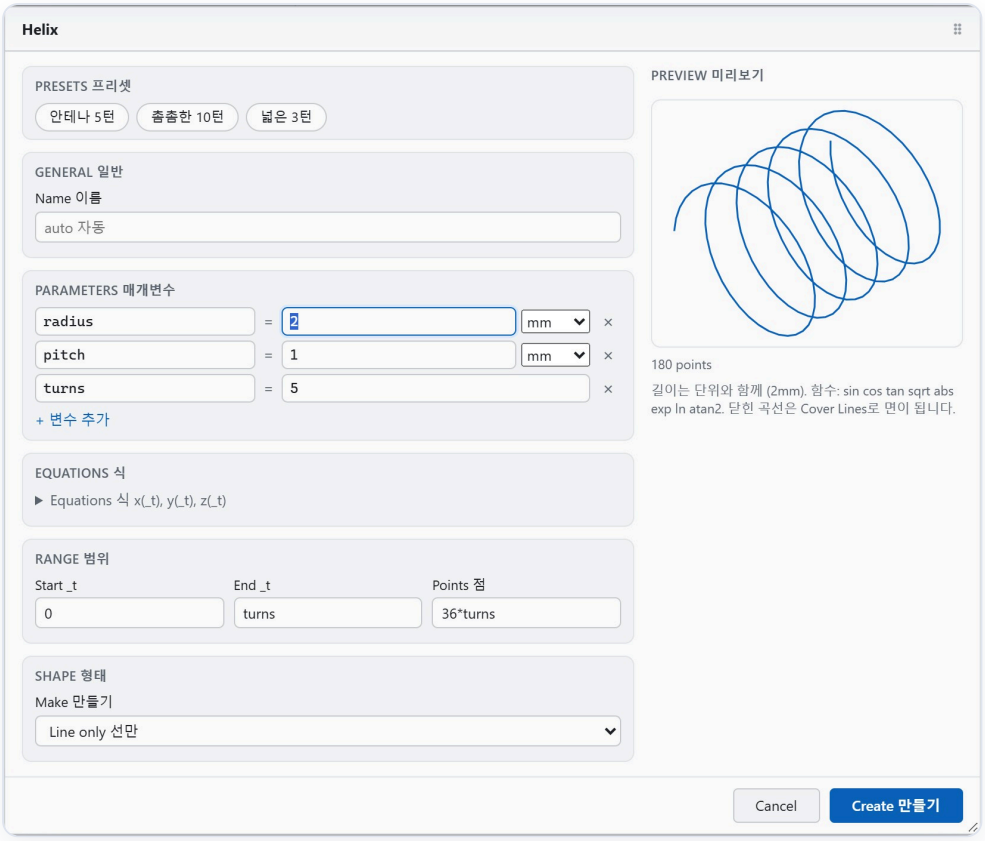


Figure 8-2 The Helix creation and preview window. Change the number of turns, radius or pitch, and the projection on the right and the 3D viewport update instantly.

PATH ONLY

Line only

A pure geometric path with no thickness or width (for sweep paths; it can't carry current on its own).

2D TRACE

Flat trace

A planar copper sheet with a specified line width (planar spiral antennas · inductors).

3D BAR

Bar

A solid conductor with a width × thickness (e.g. 35 µm) rectangular section.

WIRE

Round wire

A solid wire with a circular section (wound helical antennas · air-core chokes).

8.3 `Edit curve`: change the equation even after creation UPGRADE

After making an equation curve or spiral coil, there's no need to delete and redraw it when you want to change the number of turns or the radius. Click the object in the tree or viewport and press the **Edit curve** button in the Properties pane at the lower left: the parameters and equations you originally entered are restored exactly, and the shape is updated in place.

Closed line segments imported from DXF and the like are filled into a patch sheet with **Cover Closed Line**, and open center lines are given a line width with **Line Pattern** to turn them into conductor patterns.

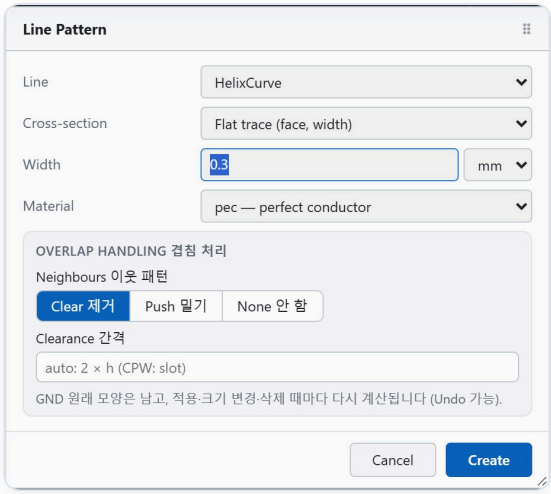


Figure 8-3 Line Pattern. It gives a center line a copper width or a round-wire cross-section.

09 CHAPTER

Practical RF PCB · Bondwires · Smart Vias · Murata Real Chips



These are the practical layout weapons that evolved most spectacularly in Desktop 2026 V2.3! Fully master JEDEC bondwires linking die and board, λg/10 automatic via fences, 54 Murata chips (.s2p) that keep their self-resonance (SRF) intact, and bidirectional butterfly stubs.

You will learn

JEDEC 4-point Bondwire and parallel wires

Try it

Automatic λg/10 Via Fill and parasitic L calculation

Key concepts

Murata .s2p real chip parts and butterfly stubs · meanders

9.1 From die pad to substrate: 3D `Bondwire` NEW V2.3

Inside bare-die MMICs and GaN transistor packages, the main culprit behind the largest series inductance ($0.7 \sim 1$ $\mathrm{nH/mm}$) is the bondwire. Press ribbon **Draw ▶ Bondwire** and click **bond pad point → lead (substrate) point** with the mouse in the 3D viewport, and a real three-dimensional loop wire is created instantly.

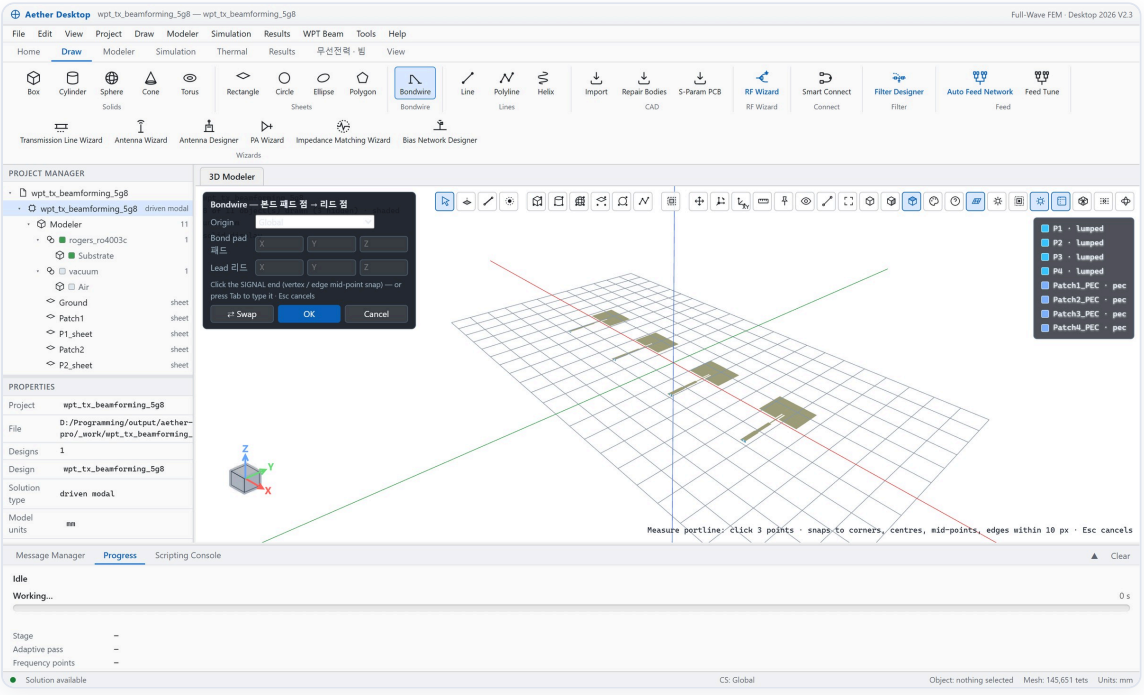


Figure 9-1 Bondwire picking mode on the Draw ribbon. It snaps automatically to vertices and edge midpoints, and the Swap button reverses the start and end.

- **Three loop profiles** — supports the practical standard **JEDEC 4-point** (rises vertically, then comes down at a slant), a smooth **Parabolic** profile, and a flat-topped **Trapezoid**; even after creation, you can re-edit the loop height and diameter in the Properties pane at any time.

- **Round wire vs ribbon & multiple parallel bonding** — besides gold / aluminum wire of $18 \sim 50\ \mu\mathrm{m}$ diameter, it creates high-frequency, low-inductance **ribbons (Ribbon, width × thickness)** and 2–8 parallel strands (`count` , `pitch`) in one go, and estimates and shows the skin-effect AC resistance R_{ac} and the equivalent inductance L.



Mesh's convergence · accuracy check

Draw a $25\ \mu\mathrm{m}$-diameter cylinder smoothly with 32 sides, and tens of thousands of tetrahedra crowd into a single wire! The Bondwire tool recommends a **6–8-sided prism cross-section** by default, which cuts the mesh count dramatically while keeping exactly the same analysis accuracy.

9.2 A 48-via fence in one click: `Via Fill / Smart Via` NEW V2.3 ONLY IN AETHER

The days of drudgery, planting vias one by one as cylinders on a ground pad or CPWG copper plate and drilling the holes in the substrate with Subtract, are over! Select the copper sheet and run ribbon **Modeler ▶ Via Fill** (**Modeler ▶ RF ▶ Via Fill / Smart Via...**).

- **Automatic frequency-based spacing rule** — it automatically recognizes the substrate below (ε_r, h) and the analysis frequency, and places a perimeter fence + inner-grid vias at a $\lambda_g/10$ spacing ($\lambda_g/20$ with the strict check) that blocks leaking waves.
- **Instant parasitic-inductance calculation** — as in the figure on the right, it calculates and shows in real time the inductance per via (550 pH) and the combined inductance of 48 in parallel (**11.5 pH!**).
- **Non-destructive grouping & automatic restoration of substrate holes** — `Group as one object` raises mesh efficiency, and when you later modify or delete the via group, the holes drilled in the substrate are filled back in without a trace!

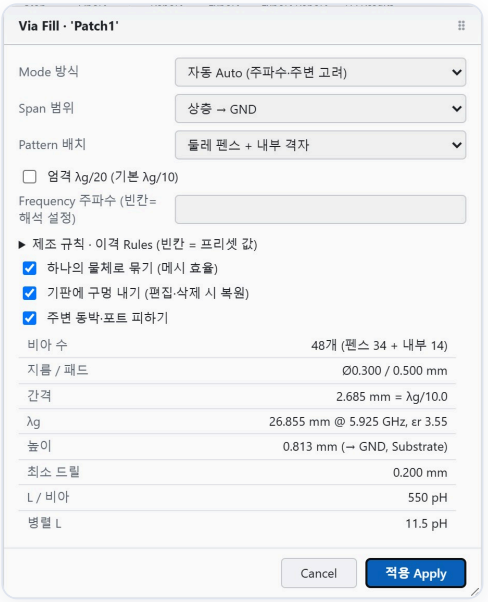


Figure 9-2 The Via Fill dialog, automatically calculating 48 vias (34 fence + 14 inner) and a parallel inductance of 11.5 pH for a patch on a 0.813 mm RO4003C substrate.

HOW TO **Pick the top-side pad, not the bottom GND! Via Fill in 4 steps**

1. **Select the top-side copper sheet**
   In the viewport (`0` mode) or the tree, click **the top-side ground island or patch sheet** where the vias will go (note: not the full bottom Ground sheet!).

2. **Open the Via Fill window**
   Press ribbon **Modeler ▶ Via Fill**, and the tool automatically reads the thickness (h) and permittivity (ε_r) of the dielectric substrate directly below, and the height of the bottom ground plane.

3. **Check the drill size · parasitic L**
   Check the `Drill diameter` (e.g. `0.3mm`) and the spacing rule (default $\lambda_g/10$), review the live-calculated total via count and **parallel combined inductance (e.g. 11.5 pH)** at the bottom, then press **Apply**.

4. **Non-destructive edit · restore**
   If you want to change the spacing, just delete the `ViaFill_*` group in the tree. Even the dozens of holes drilled in the substrate are filled back in without a trace!

9.3 Don't let the ideal C betray you: the `Murata .s2p` real chip part library

NEW V2.3

Why does a matching circuit that worked perfectly with an "ideal 2.2 pF capacitor" in a 5.8 GHz circuit go completely off once you build the real board? Because the parasitic series inductance (ESL) inside a real multilayer ceramic capacitor (MLCC) causes **self-resonance (SRF, Self-Resonant Frequency)** at a certain frequency, and above it the capacitor turns into an **inductor** instead!

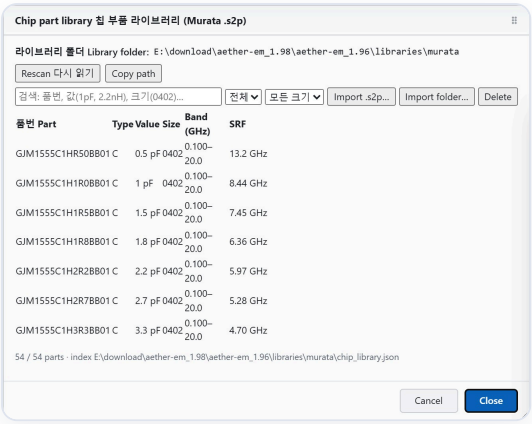


Figure 9-3 The built-in Murata 0402 (.s2p) chip part library (54 parts). It warns you at a glance that the SRF of the 2.2 pF part (GJM1555C1H2R2BB01) is 5.97 GHz, right next to the 5.8 GHz operating point!

The **SMD Part, Place SMD at Point and Lumped RLC** dialogs now include a 3-way `Model` selector.

1. **Ideal R / L / C**
   A textbook ideal element with no parasitics (for checking an initial concept).

2. **Real part (.s2p)**
   Injects the per-frequency complex impedance from the 54 built-in Murata GJM/LQP measured `.s2p` files (or vendor `.s2p` files you add) directly into the 3D EM boundary and Co-sim!

3. **Fitted circuit**
   Applies an effective series R-L-C equivalent circuit extracted from the `.s2p`.

In addition, press ribbon **SMD @ Point** to click anywhere on a meander or slanted line and place a part there. While placing it, the `R` / `Shift`+`R` keys turn it in 90° steps, and choosing parallel (shunt) also creates the ground pad and two vias automatically.

HOW TO **Click anywhere on a meander! Place a real Murata .s2p chip and check its self-resonance (SRF)**

1. **Click the position & rotate**
   Press ribbon **Modeler ▶ SMD @ Point** and click the point you want on the line. Set the direction in 90° steps with the `R` key, and choose series (`Series` , the line is cut automatically) or parallel (`Shunt` , a ground pad + 2 vias are created automatically).

2. **Switch to Real part (.s2p)**
   Change `Model` to **Real part (.s2p)**, and the catalog of 54 built-in Murata 0402/0603 GJM (capacitor) · LQP (inductor) parts opens.

3. **Check the SRF safety margin**
   After choosing the capacitance / inductance you want from the list, check that **the displayed SRF is sufficiently higher than your circuit's center frequency (1.3× or more recommended)**. If the SRF is too close, use a smaller capacitance in parallel or switch to a 0201/0402 low-ESL series.

4. **Create the 3D shape + EM boundary together**
   Press **Apply**, and the solder pads, chip body and ground vias are assembled in one go together with a full-band measured `.s2p` impedance boundary!

9.4 Free-length meanders · butterfly C/L stubs · shorted radial stubs · PCB coils

UPGRADE

Meander — the magic of the `Fix length` toggle UPGRADE

Modeler ▶ Meander... , at its default (`Fix length` on), folds the line into a zigzag while preserving the original line's total length exactly. In V2.3, **when you uncheck** `Fix length` , you can keep the span width as it is and type the target electrical length you want directly, or drag the white end-point handle up to 3× to stretch a phase-delay line freely.

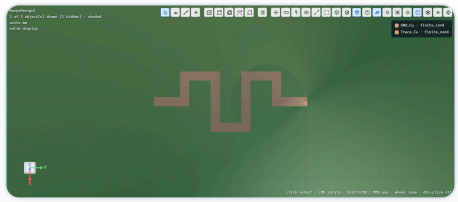


Figure 9-4 A 20 mm straight line folded into a 3-turn meander (width 10.01 mm). Now, with the length unlocked, it stretches freely to the phase length you want.

BUTTERFLY C / L

Bidirectional symmetric · asymmetric stubs NEW V2.3

RF ▶ C / L from a Line... supports **round · radial · polygon pads** besides rectangles, and placement on **Both sides** of the line **(butterfly-symmetric C/2 or an asymmetric ratio)**, halving discontinuity parasitics.

RADIAL SHORT

Shorted radial stub NEW V2.3

With Radial in **Modeler ▶ Stub...** , **shorted by vias** places a via array along the arc automatically, so the stub stays open (unloaded) in the RF band while becoming a **strong DC return and ESD discharge protection path**.

PCB HELIX

Through-substrate helical coil

Choose a dielectric board and run **PCB Helical Coil** to generate a 3D solenoid inductor wound by top and bottom traces and through vias (with the estimated L · SRF shown).

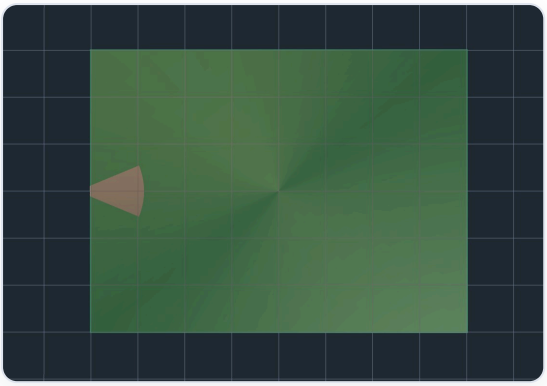


Figure 9-5 A 45° open radial stub synthesized next to a 50 Ω main line, and the FEM frequency re-tuning (Solved at retune) feature.

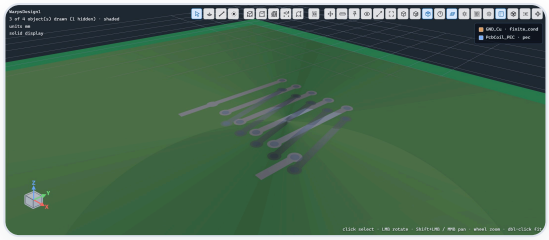
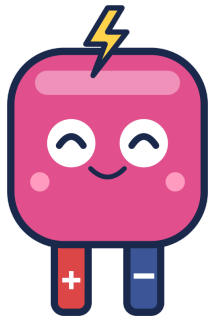


Figure 9-6 A 5-turn PCB helical coil generated automatically on a 0.508 mm substrate (about 11.2 nH, SRF 3.26 GHz).

10 CHAPTER

Automatic Copper-Overlap Cleanup (Clear · Push) and DRC Review



When you place a stub on a coplanar ground plane (CPWG) or lengthen a meander on a crowded board, don't do Boolean subtracts one by one or move neighboring lines by hand. The tool clears and pushes for you.

You will learn

The three overlap policies: Clear · Push · None

Try it

Automatic GND clearance that preserves the original

Key concepts

Automatic pushing of neighboring traces, and DRC

10.1 Three intelligent rules that kick in when patterns collide

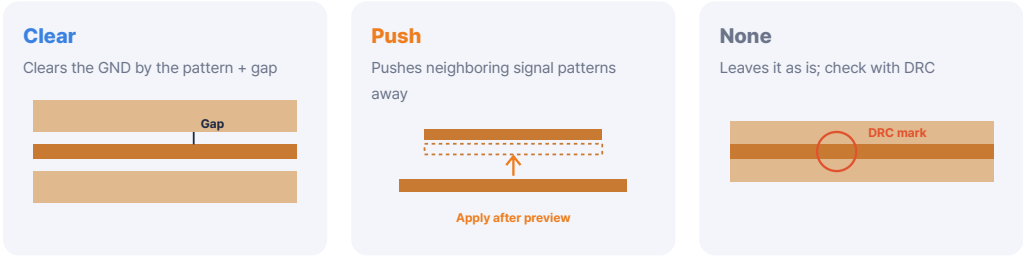


Figure 10-1 The three copper-overlap modes. Clear carves out the clearance gap while remembering the original GND, and Push shoves adjacent signal lines out beyond the safe distance.

The **Overlap & Clearance** engine is connected to the bottom of every RF pattern tool and to the right-click menu.

- **Clear (automatic GND clearing)** ONLY IN AETHER — automatically carves out the ground copper on the same layer by the specified gap (default 2 × the substrate thickness h) from the signal pattern's outline. Unlike the destructive Boolean (Subtract) of ordinary EM tools, it **remembers the original ground shape non-destructively**, so when you later delete or shrink the stub, the carved-out ground is filled back in automatically!
- **Push (automatic pushing of neighboring traces, `Push Neighbours…`)** UPGRADE — when a newly widened meander or pad gets too close to the signal line next to it, it shows a preview of moving the neighboring trace in parallel by the intrusion distance, and pushes it safely out of the way.
- **Design Rule Check (DRC)** — press **Modeler ▶ Design Rule Check (DRC)** to mark shorts (overlaps) between conductors on the same layer and violations of the minimum process gap (default 0.1 mm) with red highlights in the 3D view.

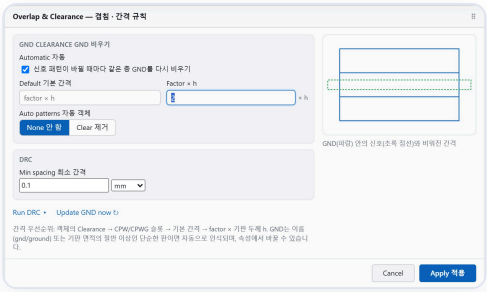


Figure 10-2 The Overlap & Clearance rule settings window. It manages automatic clearance updates and the minimum process gap.

HOW TO **Try non-destructive automatic GND clearing with the built-in sample (Overlap_Clear_Start_5G8.warp)**

1. **Open the sample & detect shorts with DRC**
   Open `Overlap_Clear_Start_5G8.warp` from **File ▶ Open Examples…**, then run **Modeler ▶ Design Rule Check (DRC)**. The shorted area where the upper CPWG ground copper and the signal stub overlap is highlighted in red.

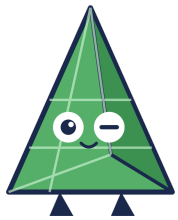
2. **Apply automatic clearance (Clear)**
   Open **Modeler ▶ Overlap & Clearance…**, leave the policy at **Clear** and the clearance gap at `0.4mm` (or `2*h`), and press **Apply**: the ground copper is carved out precisely along the stub's outline.

3. **See the non-destructive automatic restore!**
   Now select the stub and move it 1 mm to the side, or make it smaller. The ground at the new position is carved out automatically, and at the same time **the old spot that was carved out earlier is filled back in without a trace!**

4. **Pass the DRC re-check**
   Run **DRC** again and check that it shows `0 violations (PASS)`.

11 CHAPTER

Material Library and Conductor · Dispersive-Medium Modeling



Even the same 14 mm patch has a completely different resonant frequency and gain depending on whether it sits on RO4003C or FR-4. This chapter sums up the built-in RF substrate, ceramic and metal materials, and the principles of high-frequency dispersion and roughness modeling.

You will learn

A library of 40-odd standard RF · ceramic · metal materials

Try it

Frequency-dispersive dielectrics (Debye · Djordjevic-Sarkar)

Key concepts

When to choose sheet conductors vs 3D solid conductors

11.1 The Material Manager (`Material Manager`)

Project ▶ Material Manager... comes with Rogers (`RO4003C` , `RO4350B` , `RO3003/3010`), Taconic/RT (`RT/duroid 5880`), `FR-4` , high-thermal-conductivity ceramics (`AlN` , `Alumina` , `BeO`), semiconductors (`Si` , `GaN` , `SiC`) and conductors (`copper` , `gold` , `aluminum` , `silver` , `pec`) built in.

For wideband analysis, besides a constant $\tan\delta$ it supports **causal Djordjevic-Sarkar · Debye · Lorentz frequency-dispersion models**, and for finite-conductivity boundaries it includes copper surface roughness (RMS roughness, Hammerstad/Groisse correction) to prevent underestimating conductor loss at millimeter-wave frequencies.

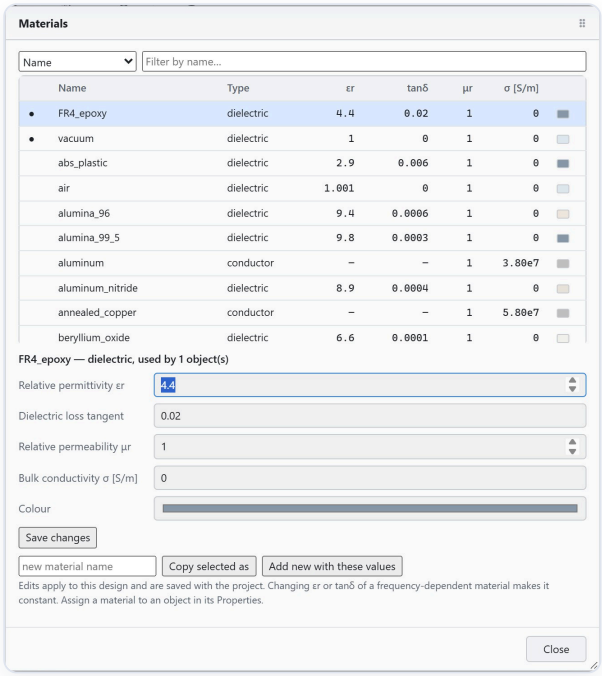


Figure 11-1 The Material Manager. Materials in use in the current design are marked with a dot (•), and they are customized safely per project.

2D SHEET

Finite-conductivity copper sheet

Captures ohmic loss accurately with a skin-impedance boundary and needs no mesh through the thickness, making it the standard for ordinary PCB analysis.

3D SOLID

Real-thickness (35 μm) solid

Use it when **sidewall field coupling** of the copper is decisive, as in tightly coupled couplers with gaps of 0.1 mm or less (the interior mesh is skipped automatically).

PEC

Perfect electric conductor

Zero resistive loss. Use it for pure radiation Q, lossless theory checks and symmetry walls.

12 CHAPTER

Fast External CAD (STEP · DXF · KiCad · Gerber) Import and Step to RF Line



Read in multilayer STEP boards drilled with hundreds of vias and DXFs mixed with NURBS curves in an instant, and promote a dumb copper lump brought in from outside into a smart RF transmission line with a single click!

You will learn

Binary-blob fast STEP · precise DXF · KiCad/Gerber import

Try it

Unit verification and automatic material mapping from layer names

Key concepts

The magic of right-click **RF ▶ Step to RF Line** promotion

12.1 An ultra-fast external CAD · PCB import engine UPGRADE

File ▶ Import ▶ reads all the major standard formats of the mechanical, circuit and artwork teams directly. In Desktop 2026 V2.3 in particular, the speed and precision of importing large assemblies took a big leap.

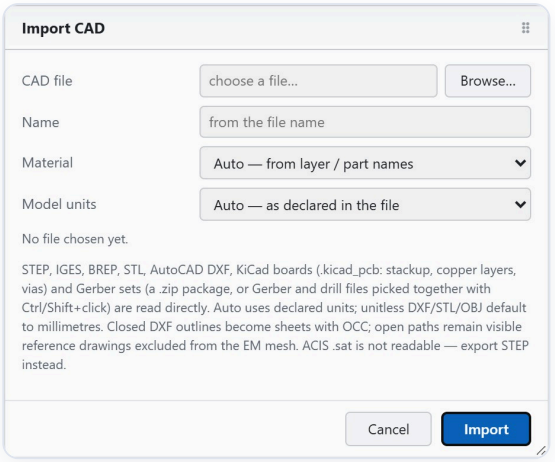


Figure 12-1 The Import CAD dialog. It verifies the real outline dimensions in mm and the body count before import, ruling out unit accidents (mm vs inch/m) from the start.

- **Faster STEP / IGES / BREP** — with OpenCASCADE parallel surface triangulation (`Fast` / `Balanced` / `Fine` presets) and a raw binary `/api/blob` hash cache, even an 80 GHz multilayer board with hundreds of vias is read without a hitch and stored, compressed, inside a single `.warp` file.
- **More precise DXF / GDSII** UPGRADE — nested blocks (`INSERT` rotation · non-uniform scale · arrays), polyline arcs (`Bulge`), `SPLINE` (NURBS), interior-hole subtraction and `$INSUNITS` units are restored precisely, and you choose to import as a **2D sheet / thickness-extruded 3D solid / polyline**.
- **KiCad (`.kicad_pcb`) · Gerber (`.zip` / drill)** — the multilayer stack thickness, copper layers (`F.Cu`, `B.Cu`) and drilled via barrels are assembled in 3D automatically, and materials are mapped automatically from part and layer names (`RO4003C`, `patch`, `gnd`).

12.2 Turn an external copper solid into a parametric line!

`Step to RF Line…` NEW V2.3 ONLY IN AETHER

When you load an external STEP or KiCad/Gerber board into other commercial EM tools, every copper trace becomes a "dumb 3D polygon lump with no history", and to change even one line width or 10° of phase you had to go back to the artwork tool. In Aether EM, it's done the moment you right-click the imported copper trace (or the face of a straight section) and press **RF ▶ Step to RF Line…** (**Edit as RF Line…** in the Properties pane)!

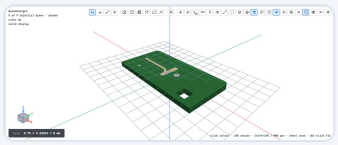


Figure 12-2 ① Right after import: a plain copper polygon brought in from KiCad/STEP (no parametric properties).

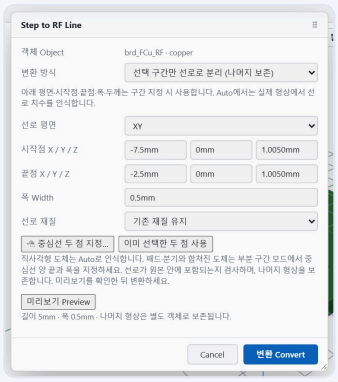


Figure 12-3 ② Step to RF Line promotion: it recognizes the substrate below automatically, reads Z0 and the electrical length, and converts with an area error of 2.5×10^{-16} mm²!

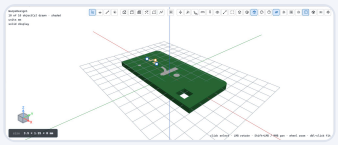


Figure 12-4 ③ Meander applied instantly: fold the promoted line into a zigzag right where it is, and the phase-delay line is done!

HOW TO **Attach stubs and meanders directly to an external STEP · KiCad trace**

1. **Right-click the trace ▶ RF ▶ Step to RF Line...**
   The tool geometrically traces back the trace's centerline and line width (area-preserving precision of $2.5 \times 10^{-16}\ \mathrm{mm}^2$!) and automatically detects the dielectric substrate directly below (ε_r, thickness h) and the position of the ground plane.

2. **Promote it to a parametric RF line**
   It instantly calculates the characteristic impedance Z_0 of the current line width, and when you enter a target Z_0 (e.g. 50 Ω), the line width is precisely corrected on the spot.

3. **Every RF tool unlocked!**
   On a promoted line, **Meander (fixed length / free stretch), Radial/Class-F Stub, C/L from Line, SMD Part and Auto Port** work exactly the same, 100 %, as on a line drawn in Aether EM from the start!

12.3 Exporting fabrication drawings (STEP · STL · multilayer DXF · glTF)

Once design and tuning are finished, the 3D shape is exported cleanly through **File ▶ Export ▶** as **STEP / STL / 3D glTF (`.glb`)** for mechanical review, or as **layer-by-layer 2D/3D DXF drawings** for PCB artwork exchange (with an option to exclude air · PML automatically).

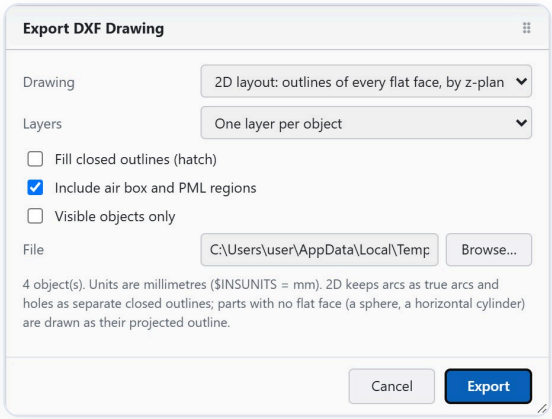


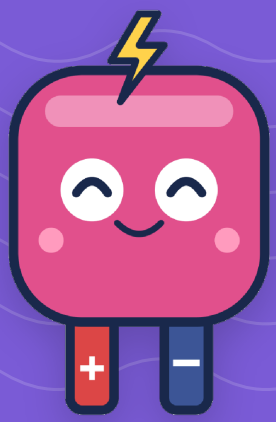
Figure 12-5 Export DXF Drawing. It offers layer separation by z-level and by material, and a hatching option for closed polygons.

PART

03

Boundaries · Ports · Fast Solver · Optimization
Getting Accurate Answers Fast

Even with the very same 3D drawing, how you set the boundary conditions, port reference planes and mesh convergence rules decides whether you get a masterpiece design or a false resonance. Part 3 covers 8 kinds of boundaries and PML open regions, how to assign ports automatically in 3 seconds, the fast reduced-order (_ProjectedROM) sweep and the fatal trap of a fixed coarse mesh, and Optuna Bayesian (TPE) optimization, which finds the optimal dimensions with the fewest FEM runs.



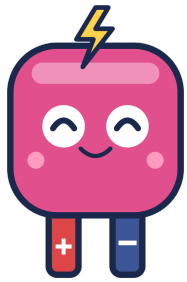
13 Mastering Boundary Conditions · Open Regions (Radiation/PML) · Ports

14 Solution Setup · Adaptive Mesh · Fast Frequency Sweep

15 Validation · Running · Eigenmode · Optuna Bayesian Optimization

13 CHAPTER

Mastering Boundary Conditions · Open Regions (Radiation/PML) · Ports



Boundary conditions give physical laws to the outer edge of the analysis space and to conductor surfaces, and ports are the gateways through which RF energy goes in and out. Learn three shortcuts for setting up an accurate port in 3 seconds, with no polarity mistakes.

You will learn
8 core boundary conditions and Lumped RLC

Try it
Choosing between Radiation and PML open regions

Key concepts
Wave Port · Lumped Port · Auto Port and polarity

13.1 Eight boundary conditions that set the rules of the analysis space

Assign them with **Simulation ▶ Assign ▶ ▶ Boundary...**, or by selecting a face (F) and right-clicking.

Boundary type	Physical meaning	Typical use · default
Perfect E (PEC)	Tangential E-field $\mathbf{E}_t = 0$ (lossless perfect electric wall)	Ideal ground plane, waveguide outer wall
Perfect H (PMC)	Tangential H-field $\mathbf{H}_t = 0$ (ideal magnetic wall)	Even-symmetry plane, open-end approximation
Finite Conductivity	Includes skin effect + copper thickness + surface-roughness ohmic loss	Real copper · gold · aluminum conductor sheets
Radiation	First-order spherical-wave absorbing boundary (approximates open free space)	Outer faces of an ordinary antenna air box
Impedance	Uniform surface sheet resistance · reactance $Z_s = R + jX$ [Ω/sq]	Thin-film resistors, EM absorber sheets (377 Ω/sq)
Lumped RLC UPGRADE	Lumped $R \cdot L \cdot C$ across the two ends of a sheet, or a **real Murata chip (.s2p)**	SMD matching elements, 50 Ω termination resistors, bias decoupling
Symmetry E / H	Declaring an electromagnetic symmetry plane cuts the solved volume to 1/2 or 1/4	Symmetric horn antennas, cavity resonators, differential pairs

Always check that a boundary isn't floating in thin air

If a name appears in the legend at the upper right but the number of triangles it covers is 0, a warning appears in the Message Manager. Right after a Boolean edit, make a habit of clicking the legend entry to check that the face you want is highlighted; it will save you hours of re-analysis.

Q&A **The `Parallel` checkbox in the Lumped RLC dialog: should it be on or off?**

When you enter the parasitics of a real chip capacitor (MLCC), you must leave it unchecked (series connection)! A real bypass chip (e.g. $R = 0.1\ \Omega$, $L = 0.4$ nH, $C = 100$ pF) is a **series resonant circuit** ($Z = R + j\omega L + 1/(j\omega C)$, a short-circuit pass near 0.8 GHz!) in which the current flows through `ESR → ESL → C` in turn. If you check `Parallel` without thinking, the three elements are connected side by side in parallel and turn into a single 0.1 Ω resistor, or into the exact opposite: a parallel anti-resonance trap. Turn `Parallel` on only when modeling a parallel-resonant LC tank circuit.

13.2 Creating open free space: Radiation vs PML

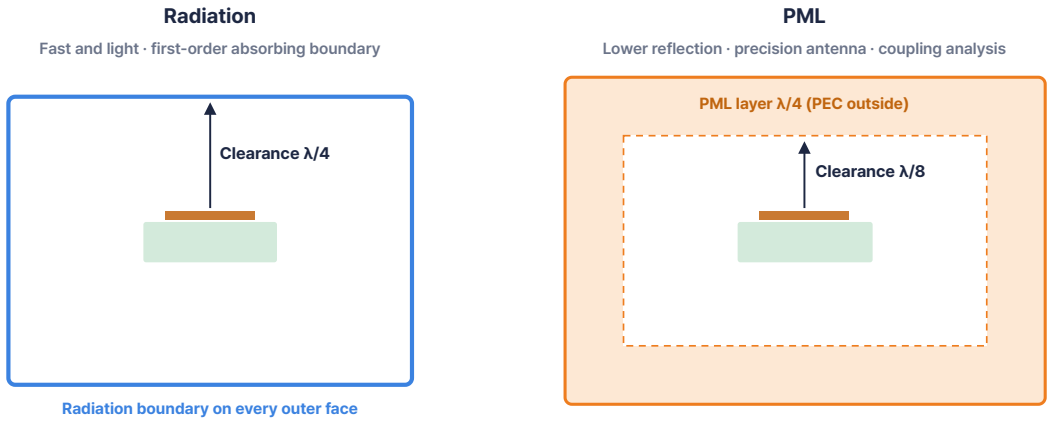


Figure 13-1 Comparison of the Radiation boundary (λ/4 air clearance + first-order absorbing face) and the PML perfectly matched layer (λ/8 clearance + λ/4 anisotropic absorbing layer + PEC outer wall).

Structures that radiate waves into space, like antennas, must be wrapped with **Simulation ▶ Open Region (Radiation / PML)...**. Enter just the lowest frequency of the band, and it calculates the wavelength λ_0 and generates the air box automatically.

- **Radiation** — $\lambda_0/4$ clearance from the structure. Light and fast, and enough for ordinary patch and dipole designs.
- **PML (recommended for high precision)** — after a $\lambda_0/8$ clearance from the structure, it places a perfectly matched absorbing layer $\lambda_0/4$ thick. Even for beam-steering arrays with oblique incidence or high-gain antennas, reflection is suppressed to -50 dB or below.

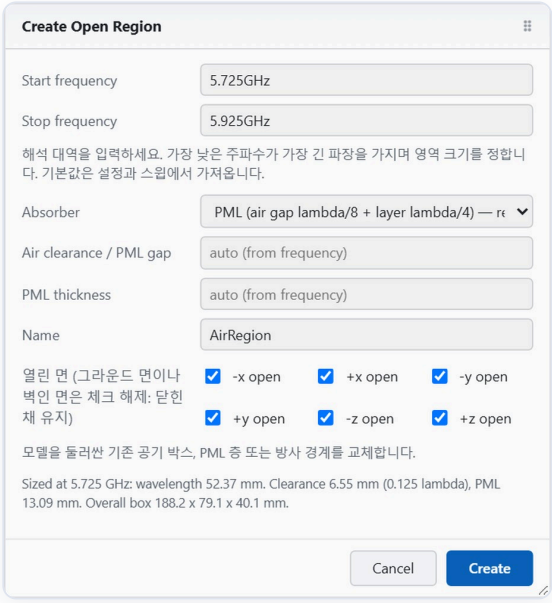


Figure 13-2 The Create Open Region dialog. For a patch antenna whose ground plane closes off the bottom, unchecking the −Z direction saves unnecessary air mesh underneath.

13.3 Wave Port vs Lumped Port — when to use which?

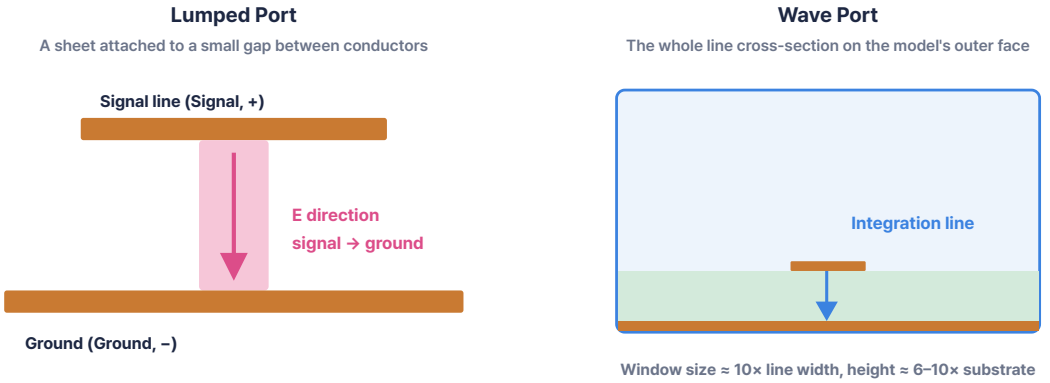


Figure 13-3 A Lumped Port placed in a narrow feed gap inside the model, and a Wave Port covering the whole cross-section of the analysis region's outer wall.

Type	Lumped Port	Wave Port (waveguide-mode port)
Location	A small gap ($< \lambda/10$) between the signal conductor and ground **inside** the model	A line cross-section window touching the analysis air box's **outer boundary face**
How it works	Applies a uniform E-field to the port sheet, normalized to a user-specified Z_0 (usually 50 Ω)	First solves a 2D cross-section eigenvalue problem, then excites with the real TEM/TE/TM mode field distribution
Strengths · uses	Inset patches, dipole centers, transistor gate/drain internal terminals	Waveguides, coaxial connectors, precision microstrip · CPWG inputs/outputs, reference-plane de-embedding

13.4 Three ways to attach a port in 3 seconds without mistakes

1. **Port (pick): one-click sheet creation**
   Press ribbon **Home ▸ Port (pick)**, then **click the signal end face → click the ground face → press Apply**, and a sheet that exactly fits the gap is created and assigned as a port in one go.

2. **Port Marks ▸ Auto Port**
   Right-click a conductor or face and mark it with **Mark as Signal (+)** and **Mark as Ground (−)**, then choose **Auto Port ▸ Assign Port (auto type)**: it decides between Wave and Lumped on its own, based on whether it touches the outer boundary, and creates the port.

3. **Verify the polarity**
   The integration-line arrow always points **from Signal (+) to Ground (−)**. If the phase is flipped by 180° in a differential array or divider, right-click the port and choose **Reverse Polarity** to fix it instantly.

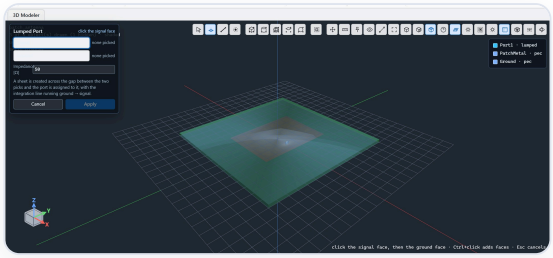


Figure 13-4 The Port (pick) helper at the upper left of the viewport, and the Assign Lumped Port settings.

HOW TO **The window-size formula for a precise microstrip Wave Port ($8W \times 6h$) and 4-step setup**

1. **Check contact with the outer wall**
   Check that the end of the microstrip line and the bottom ground plane meet the outer boundary face of the analysis air box (`AirBox`) with no gap (if they are inside the model, use a `Lumped Port`).

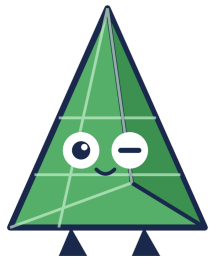
2. **Draw the port window sheet (the $8W \times 6h$ golden ratio)**
   Draw a rectangular sheet on the air box's outer-wall plane. The standard is **a width of $6 \sim 10\times$ the signal line width** and **a height of $5 \sim 6\times$ the substrate thickness** upward from the bottom ground plane. (If the window is too narrow, the fringing E-field is cut off and Z_0 goes off; if it's so large that it covers the whole air box, waveguide higher-order modes creep in!)

3. **Assign the Integration Line**
   Select the port sheet, open **Simulation ▶ Assign ▶ Wave Port...**, and click the integration line's start point at **the center of the bottom ground plane** and its end point at **the center of the signal line**, to set up a vertical arrow.

4. **Check the mode impedance**
   After the analysis, open **Results ▶ Port Modes** and check that the characteristic impedance Z_0 of the extracted fundamental quasi-TEM mode is close to the intended $50 \pm 1\ \Omega$.

14 CHAPTER

Solution Setup · Adaptive Mesh · Fast Frequency Sweep



We dissect how the adaptive mesh works, in which the FEM solver splits the mesh by itself where the error is large and closes in on the right answer, and the reduced-order (_ProjectedROM) engine, which speeds up sweeps several-fold with zero accuracy loss (|ΔS| = 0).

You will learn

Adaptive passes and basis order (Zero · First · Mixed)

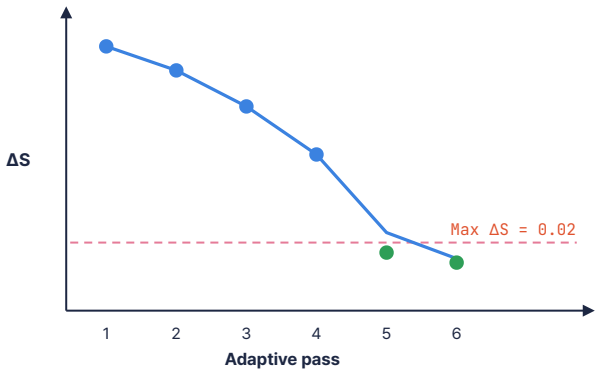
Try it

The fatal trap of a fixed coarse mesh (a −33.7 dB illusion!)

Key concepts

Discrete · Interpolating · Fast (_ProjectedROM) sweeps and parallel workers

14.1 Adaptive Mesh and basis-function order



Convergence check

Stops when passes with ΔS below the criterion occur 2 times in a row (default)
Zero order needs at least 3 passes

A fixed coarse mesh risks false resonances!

Figure 14-1 The adaptive-mesh refinement loop. It selectively splits only the corner tetrahedra where the E-field energy error is concentrated, and judges convergence when |ΔS| < the threshold for 2 consecutive passes.

The first value to take care of in **Simulation ▶ Add Solution Setup...** is the **Solution frequency**. If you leave the default of 10 GHz and run a 2.45 GHz antenna, the mesh becomes finer than it needs to be, or, conversely, too coarse for a 28 GHz circuit. **Always set it to the design center frequency (or the highest operating frequency).**

For the basis order, it supports **First order** (20 degrees of freedom per tetrahedron, the recommended default) and a **Mixed** mode that automatically places higher-order elements only around conductors and dielectrics with strong field energy. To prevent an accidental early stop, the convergence check requires **at least 2 consecutive passes** to come in at or below the $|\Delta S|$ tolerance (default 0.02).

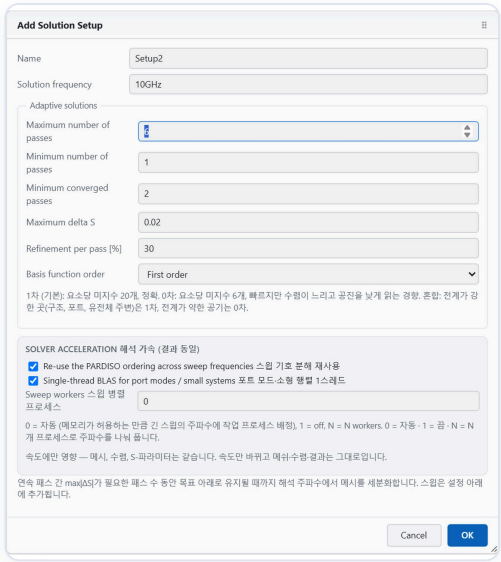


Figure 14-2 The Add Solution Setup dialog. The acceleration options at the bottom (such as reusing the PARDISO symbolic factorization) only raise the speed, without changing the result by a single bit.

CREW COMIC **A true-story warning — the disaster that followed turning off adaptive passes and running just 1 coarse-mesh pass!**



Porty Mesh! I ran the adaptive pass just once to get a quick look, and the 5.8 GHz GaN PA input match came out at **S11 = −33.68 dB**! Amazing, right?!

Mesh Stop!! That's a pure **coarse-mesh numerical illusion (coarse-mesh artifact)**! The fringing E-field at the stub corners got smeared out, and the reflection just happened to look like zero!





Wiz Right. When I solved that board (CGH40010 v1) properly again with a 10-pass converged mesh (26,563 tetrahedra), the real S11 was **−3.35 dB (more than half reflected!)**. Be sure to check the measured graphs below with your own eyes!

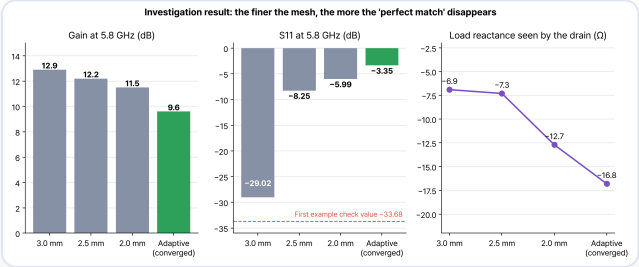


Figure 14-3 Coarse 1 pass (dotted, −33.68 dB fake jackpot!) vs 10-pass converged FEM (solid, −3.35 dB, the real thing).

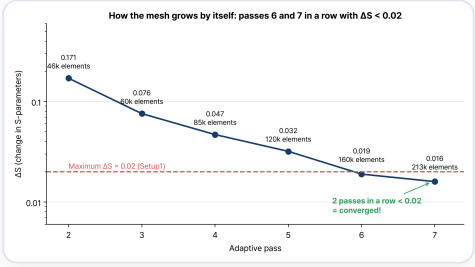


Figure 14-4 Tetrahedron count per pass and the $|\Delta S|$ convergence path. You can trust it only after it comes in below the tolerance for 2 or more consecutive passes.

14.2 The three frequency sweeps and the `_ProjectedROM` fast engine

UPGRADE

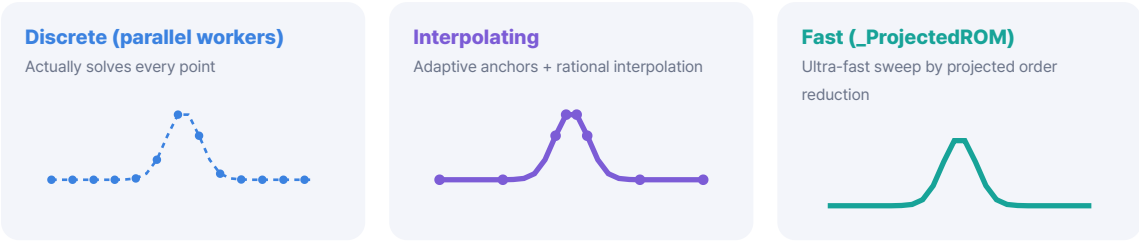


Figure 14-5 The three frequency-sweep methods compared. Fast (_ProjectedROM) and Interpolating (AAA) reconstruct a continuous response of hundreds of points from analyses at only a few anchor frequencies.

- **Fast (`_ProjectedROM` projected order reduction)** UPGRADE — uses the solution vectors found at a few anchor frequencies as an orthogonal basis (orthogonal subspace) and projects the huge FEM stiffness and mass matrices onto a reduced matrix of a few dozen dimensions. Because it adaptively adds basis vectors at the frequency with the largest residual, it draws sharp multi-resonance filters and wideband sweeps several times faster.
- **Interpolating (adaptive AAA rational interpolation)** — probes both band edges and the midpoint, concentrates samples in the sections that change sharply, and converges to within $|\Delta S| < 10^{-3}$.
- **Discrete + parallel sweep workers (`Sweep workers`)** — solves every specified frequency point independently. It is essential when you turn on **Save fields** to store per-frequency far-field and thermal-loss distributions, and multicore parallel workers calculate several frequency points at the same time.

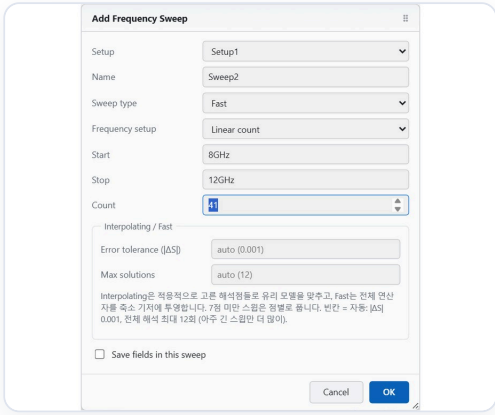


Figure 14-6 The Add Frequency Sweep dialog. A coarse Discrete sweep whose step exceeds 5 % of the band automatically raises a missed-notch warning.

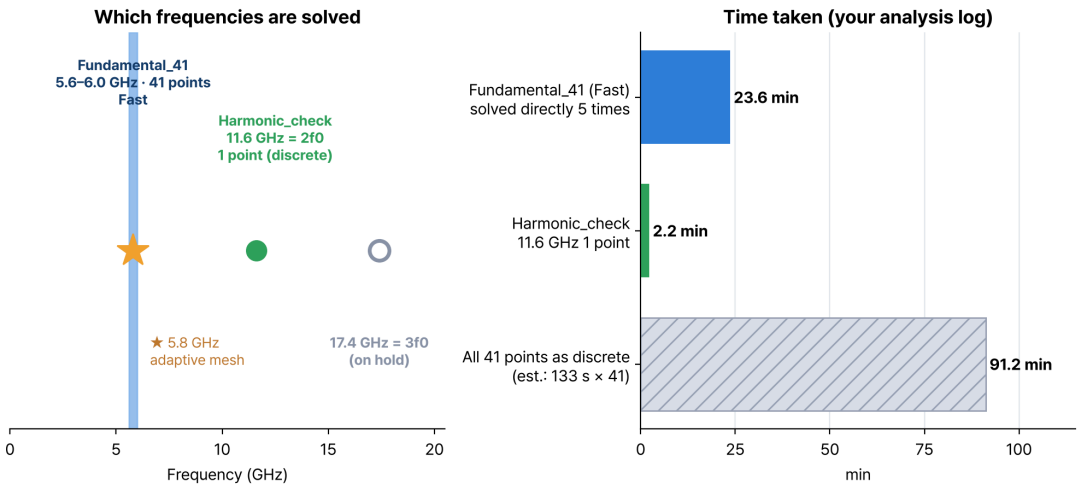


Figure 14-7 A practical multi-sweep strategy (CGH40010 board): the 41 points of the fundamental band are done with Fast (_ProjectedROM) in just 5 matrix factorizations (left), and the 2nd harmonic (11.6 GHz) is pinpointed exactly with a 1-point Discrete sweep (right)!

An expert's time-saving trick: combine a `Fast` band sweep with a `1-point Discrete` harmonic sweep!

On a 5.8 GHz PA, don't sweep the whole 5.6–12 GHz range in one go just to see both the fundamental band (5.6–6.0 GHz, 41 points) and the $2f_0$ (11.6 GHz) impedance! Register two sweeps under a single `Setup1`: ① `Fundamental_41` (**Fast sweep — only 5 of the 41 points are actually solved!**) and ② `Harmonic_check` (**Discrete sweep — the single point `11.6 GHz`**), and **with just 6 FEM matrix solves** you get both the band curve and the harmonic phase.

14.3 No more blank-field worries! Standard `Solution Setup & Sweep` recipes by design purpose

If you're at a loss for what numbers to enter when you first open the setup window, just follow and enter the verified practical standards below.

Design target	Solution Freq	Max Passes / $\lvert\Delta S\rvert$	Recommended Frequency Sweep combination (key check points)
Single · array antennas	Center frequency f_0	`12` passes / `0.02`	Band **Fast (101 points)** + center point f_0 1-point **Discrete** (`Save fields` **on — for 3D radiation patterns!)**
Filters · stubs · dividers	Top of passband f_{high}	`14` passes / `0.01`	Band **Fast (`_ProjectedROM`)** 201–401 points (loss-free reconstruction of sharp attenuation poles and notches)
Rectifiers · harmonic Co-sim	$2f_0$ (to secure a harmonic-ready mesh)	`12` passes / `0.015`	$0.5f_0 \sim 3.5f_0$ wideband Fast, or f_0, $2f_0$, $3f_0$ 3-point **Discrete** (feeds HB harmonic balance directly)
High-power PA + thermal coupling	Center frequency f_0	`12` passes / `0.015`	Band Fast + operating point f_0 1-point **Discrete** (`Save fields` **is mandatory — extracts the** `RF Loss → Heat` **heat source!)**

15 CHAPTER

Validation · Running · Eigenmode · Optuna Bayesian Optimization



Once you've gone from F5 validation through F9 running to eigenmode analysis of a cavity resonator, it's time to hand dimension tuning over to the computer. This chapter covers Optuna Bayesian (TPE) surrogate optimization, which finds a multivariable optimum with just 15–25 FEM runs.

You will learn

F5 Validation · F9 background run · keeping partial results

Try it

Spurious-free Eigenmode resonance and Q analysis

Key concepts

Parameter Study and Optuna Bayesian (TPE) goal optimization

15.1 Local mesh refinement · F5 check · F9 non-blocking run

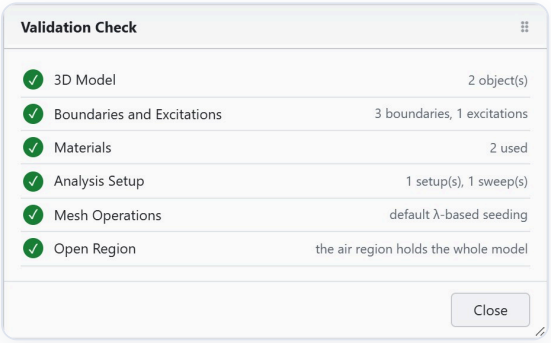


Figure 15-1 Validation Check (F5). When all 6 gates (model, boundaries, materials, setup, mesh, open region) are green, you're ready to go!

Where the field changes sharply, such as a port feed gap or a 0.15 mm coupled-line spacing, set a maximum edge length in advance with **Simulation ▶ Assign ▶ ▶ Mesh Operation...** to help the very first passes capture the field accurately.

Press F9 **Analyze All**, and the solver runs in **an independent low-priority process** separate from the UI, driving the MKL PARDISO accelerator. If you press Stop (Shift + Esc) during the analysis, the passes and frequency points finished so far aren't lost: they remain intact as **partial results (Partial Results)**, so you can plot a graph right away!

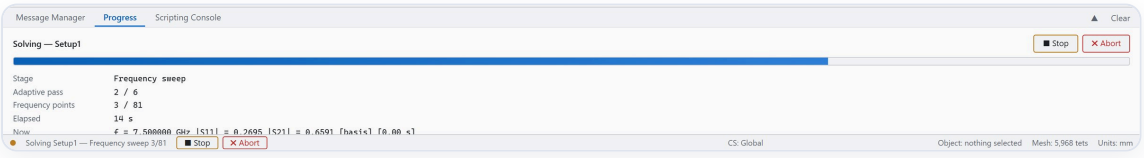


Figure 15-2 The real-time Progress dock. It shows the elapsed time for each stage and the tetrahedron and unknown counts, and any open report graph updates as if alive each time a point is solved.

15.2 Eigenmode: extracting resonant frequencies and Q_0 without ports, with `Eigenmode`

Dielectric resonators (DRA), waveguide cavity filters and wireless-power cavity resonators (Ch. 26) are analyzed with **Project ▶ Insert Eigenmode Design**. By mathematically projecting out the curl-free electrostatic nullspace, it computes, in one go and with no spurious numerical modes (spurious modes) near 0 Hz, the pure electromagnetic eigenmodes f_1, f_2, … and the unloaded Q_0 including wall and dielectric losses.

15.3 Hitting the answer with the fewest FEM runs: `Bayesian (Optuna TPE)` optimization NEW V2.3

Solving an antenna or matching circuit with 3–5 variables by grid search takes hundreds of heavy 3D FEM runs. Besides local search (Nelder-Mead, Pattern, L-BFGS-B) and global evolution (Differential Evolution), **Simulation ▶ Optimization…** in Desktop 2026 V2.3 now carries **Optuna-based Bayesian surrogate optimization (`Bayesian / TPE`)**!

- **How the Tree-structured Parzen Estimator (TPE) works** — from the handful of FEM results run so far, it updates a probability-density model of the "promising region most likely to reach the goal" each round and picks the next dimensions to try. It usually reaches an excellent optimum **within just 15–30 FEM runs**.
- **6 one-sided Hinge goal costs** — combine goals such as maximum in-band $|S_{11}| \le -15$ dB, minimum $|S_{21}| \ge -0.5$ dB, resonant notch frequency match, eigenmode frequency match and far-field peak gain. **The cost of an item that has already beaten its goal drops to 0 immediately, so the moment every goal is met, it stops smartly without using up the remaining runs!**
- **Original protected & one-click apply** — every trial runs on a temporary copy, and the result is applied to your design variables only when you press **Apply best** after it finishes (restorable with one Undo).

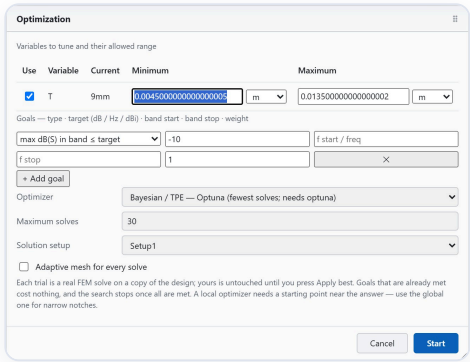


Figure 15-3 The Optimization dialog. Set the variable ranges and one-sided Hinge goals, then auto-tune with the Bayesian (Optuna TPE) or Nelder-Mead algorithm.

Search tool · algorithm	Recommended variables	When is it the fastest choice?
Solved at / Auto-tune ONLY IN AETHER	1–2	When a stub notch or patch resonance is off by 1–4 % — **a direct hit with just 1–2 FEM runs!** (Ch. 20 · 34)
Parameter Study	1–2 (grid)	When you want to see a variable's sensitivity trend ($\partial f_0/\partial L$) at a glance as a bundle of evenly spaced curves

Search tool · algorithm	Recommended variables	When is it the fastest choice?
Nelder-Mead / Pattern	2–3	When the wizard's starting values are already near the answer and you want to slide quickly down a smooth local valley
Bayesian (Optuna TPE) NEW V2.3	**3–6 (multivariable)**	When you want to find a multi-resonance · wideband global optimum while **keeping expensive 3D FEM runs to within 15–30**

HOW TO **Run Optuna auto-optimization all the way through in 5 steps with the built-in sample (slab_matching_parametric.warp)**

1. **Open the parametric sample**

   Open `slab_matching_parametric.warp` from **File ▶ Open Examples...** (if you open **Project ▶ Design Variables**, you'll see that the waveguide matching-slab thickness variable `T` is registered).

2. **Launch the optimization window**

   Click **Simulation ▶ Optimization...** in the top menu.

3. **Set the range of the tuning variable**

   Check variable `T` in the **Variables** list and set the search lower bound (`Min`) and upper bound (`Max`) (± 40 % of the default value recommended).

4. **Set the goal (Goal) & algorithm**

   In **Goals**, press **+ Add Goal** and enter `S(1,1) dB ⩽ -25 dB` (target band / frequency), set the algorithm to **Bayesian (Optuna TPE)** and the maximum number of evaluations to `20`, then press **Start**.

5. **Early stop & apply the optimum**

   When the real-time cost graph touches `0` and the run stops automatically on reaching the goal, check the optimal dimensions on the right and press **Apply best** to commit them to your 3D model!

PART

04

Reading Simulation Results Easily · Publication-Grade Reports From One Line of a Graph to the Physical Cause and the Fix

The colorful curves and rainbow-colored 3D pictures you get after pressing the simulation button are a precise diagnosis that tells you "what broke, where, why, and what to fix". Part 4 guides you step by step, from interpretation formulas that let even beginners see through the meaning of S-parameters, Smith charts, convergence tables, 3D EM fields and radiation patterns in 30 seconds, to the double-click modeless ✎ Edit publication-grade chart editor, standard-free 3-Line de-embedding and SPICE macromodel extraction.



16 How to Read S-Parameters · Smith Charts · Convergence Tables, and AePlot

17 Reading 3D E-Field · H-Field · Surface Current and Far-Field Radiation Patterns Easily

18 3-Line De-embedding · Vector Fit SPICE · Sharing with the 60 fps 3D Viewer

16 CHAPTER

How to Read S-Parameters · Smith Charts · Convergence Tables Easily, and AePlot



What percentage of the power got through when S11 is −10 dB? What part is the top half or the bottom half of the Smith chart asking you to add? Learn the physics mental math that lets you read results 100 %, together with how to edit publication-grade AePlot reports.

You will learn
The S11 · S21 dB report card and 3-second energy-conservation mental math

Try it
The Smith chart's four-direction compass and phase · group-delay analysis

Key concepts
Convergence-table · port-mode health checks and ✎ Edit paper charts

16.1 A 30-second feel for S-parameters (S_{11}, S_{21}) & the decibel (dB) pass/fail report card

At high frequencies, instead of voltage and current, we grade by **"how much of the wave bounces back (S_{11}) and how much gets across (S_{21})"**. Of the wave launched into port 1 (a_1), the fraction of reflected wave that comes back is S_{11} **(reflection coefficient)**, and the fraction of transmitted wave that exits through port 2 is S_{21} **(transmission coefficient / insertion loss · gain)**.



Port 2 terminated in a matched load, with only port 1 excited

Figure 16-1 The physical definition of 2-port S-parameters. The lower S11 is (the more negative), the less reflection and the better; for passive circuits, the closer S21 is to 0 dB, the lower the loss and the better.

S_{11} value [dB]	Reflected power ($\lvert S_{11}\rvert^2$)	Accepted power ($1 - \lvert S_{11}\rvert^2$)	Practical verdict · what it means
`-3 dB`	50.1 % reflected	49.9 % accepted	**Fail** — half the power you send bounces straight back (VSWR 5.85)
`-6 dB`	25.1 % reflected	74.9 % accepted	The compromise floor for tiny wearable · phone-embedded antennas (VSWR 3.0)
`-10 dB` ★	**10.0 % reflected**	**90.0 % accepted**	**The standard pass line for general antennas and RF modules!** (VSWR 1.92 ≈ 2:1) — the baseline for bandwidth

S_{11} value [dB]	Reflected power ($\lvert S_{11}\rvert^2$)	Accepted power ($1-\lvert S_{11}\rvert^2$)	Practical verdict · what it means
`-15 dB`	3.2 % reflected	96.8 % accepted	**Excellent match** — recommended for base-station array antennas · LNA/PA inputs and outputs (VSWR 1.43)
`-20 dB`	1.0 % reflected	99.0 % accepted	**Premium match** — the level of instruments · precision filters · calibration boards (VSWR 1.22)
`-30 dB`	0.1 % reflected	99.9 % accepted	The level of ultra-precision waveguide · coupler isolation (VSWR 1.07)

An expert's 3-second energy-conservation mental math: where did the missing power go?

In a passive 2-port circuit, $|S_{11}|^2+|S_{21}|^2+P_{\text{loss+radiation}}=1\ (100\ \%)$ always holds. For example, is a 1:2 Wilkinson power divider faulty if it shows $S_{11}=-25\ \text{dB}$ (0.3 % reflected) and $S_{21}=S_{31}=-3.30\ \text{dB}$? No! When the power splits in half, the lossless theoretical value is already $-3.01\ \text{dB}$ (50 %), so the real substrate and copper heat loss is only 0.29 dB: an excellent design. Conversely, even if a 1-port antenna shows $S_{11}=-25\ \text{dB}$, it only means "99.7 % of the power went into the antenna"; whether that power went out as radio waves or burned up in resistance must always be checked with **Realized Gain** in Ch. 17!

16.2 The Smith Chart: a 30-second compass to escape beginner level

If a Cartesian graph ($|S_{11}|$ dB) only tells you the result "it isn't matched", **Results ▶ Create Smith Chart Report** is a magic map that instantly gives you the prescription too: **"should I add an inductor (L) or a capacitor (C)?"**

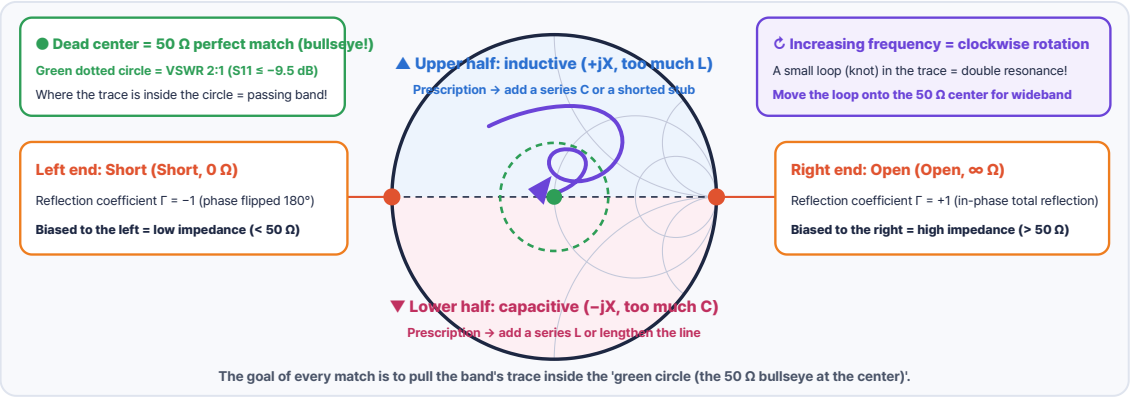


Figure 16-2 The Smith chart's four-direction compass. Take the 50 Ω at the center as the bullseye: the top is inductive (+jX), the bottom capacitive (–jX), the left a short (0 Ω), and the right an open (∞ Ω).

PHASE ∠S21

How to read phase linearity

When a signal passes through a line, the phase must fall at a constant slope proportional to frequency for the waveform to stay intact. Check that the difference between two divider ports, `∠S21 - ∠S31`, is flat at 0° (in phase) or $90^\circ/180^\circ$ (hybrid/balun).

GROUP DELAY

How to read group-delay ($\tau_g = -d\phi/d\omega$) distortion

The real propagation arrival time (ns), obtained by differentiating the phase slope. The flatter it is across the band, the cleaner wideband modulation (Wi-Fi/5G/radar chirp) waveforms are; if a sharp spike rises at a filter edge, signal ringing (worse EVM) occurs.

16.3 A 10-second health check before trusting the results: `Convergence` and `Port Modes`

Trusting a pretty graph the moment it appears can get you into big trouble (remember the -33.7 dB coarse-mesh illusion in Ch. 14!). First pass the two health checks below, which take just 10 seconds.

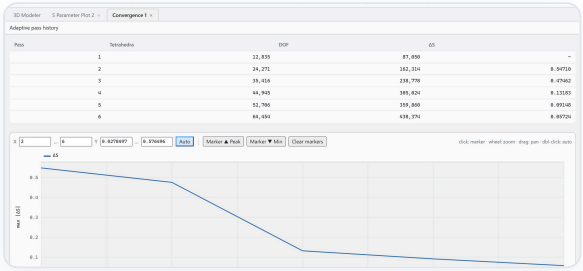


Figure 16-3 Health check ① Convergence: check that, as the tetrahedron count grows, the max|ΔS| curve (blue) settles steadily below the red reference line (0.02).



Figure 16-4 Health check ② Port Modes: check that the port characteristic impedance (Z_wave / Z_port) is near the intended 50 Ω and that there are no unwanted higher-order modes.

- **How to read Convergence** — if `max|ΔS|` comes down below the criterion for the last 2 passes in a row and flattens out, **convergence passes**. If it has gone all the way to the maximum pass (e.g. Pass 10) and still ends high, like `max|ΔS| = 0.08`, the mesh is still insufficient, so raise `Max passes` to `15` in the setup and continue solving.
- **How to read Port Modes** — if you drew a 50 Ω microstrip Wave Port but `Z_port` shows `18 Ω` or `110 Ω`, either the line width was miscalculated or the port window size is wrong. Also, if you see a second guided mode whose `f_c [GHz]` falls inside the operating band, narrow the air box or place the via fence more densely to block the parasitic box mode.

16.4 Publication-grade `AePlot` reports · the modeless `✎ Edit` editor · `Accumulate` history comparison NEW V2.3

Every 2D chart in Desktop 2026 V2.3 runs on the **integrated AePlot engine** in matplotlib publication style, and shows automatic passivity (`passive`) and reciprocity (`reciprocal`) check badges at the upper right. **Double-click** a chart or press ✎ **Edit plot**, and a modeless editor opens that lets you style it in real time without closing the window.

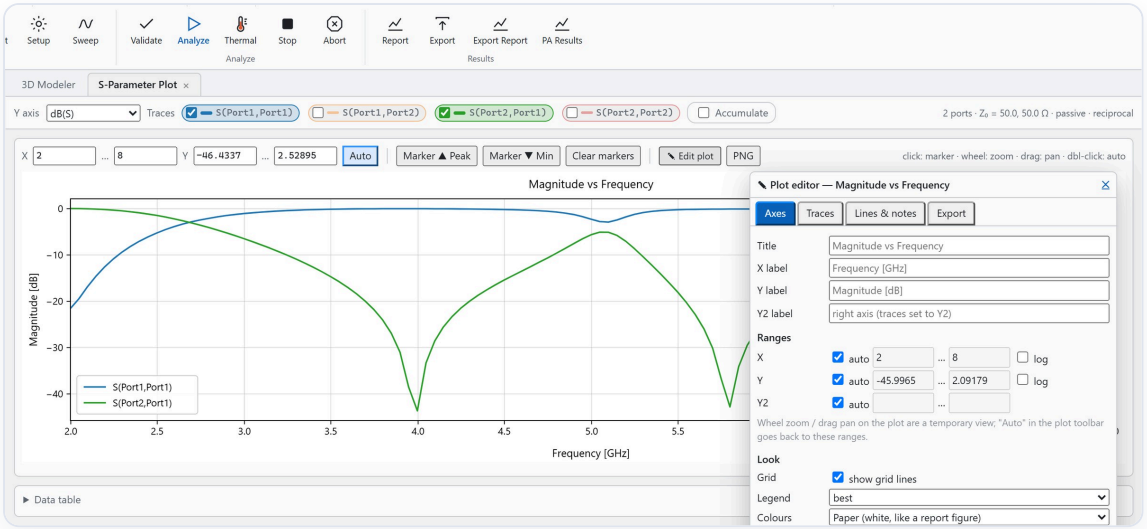


Figure 16-5 The S-parameter report of a radial-stub notch filter and the modeless Plot Editor (✎ Edit). Changes to the axis ranges, the right-hand Y2 secondary axis and arrow annotations are reflected in the chart immediately.

Results ▸ S-Parameter Metrics... precisely interpolates and extracts the lower and upper frequencies at a reference line (e.g. -10 dB) and the matching bandwidth (MHz, %). And if you turn on **Accumulate** at the top of the chart, every time you change a dimension and re-analyze, the earlier curves stack up as translucent overlays, so you can compare at a glance whether your tuning is heading the right way.

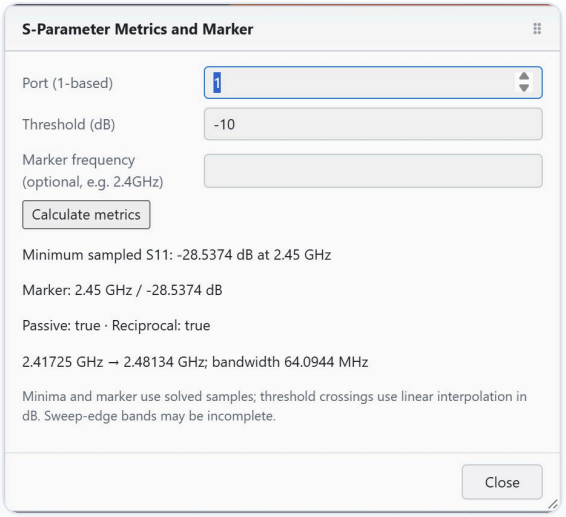


Figure 16-6 The S-Parameter Metrics window. It automatically measures the –10 dB bandwidth (64.1 MHz) and whether passivity passes.

HOW TO **A paper- or report-ready S-parameter chart in 1 minute & overlaying before and after tuning**

1. **Create the report & lock in the history**

   Press ribbon **Results ▶ S-Parameters** to bring up the graph and check **Accumulate** at the top (from the next analysis on, the earlier curves are kept automatically!).

2. **Place a marker and promote it to an arrow note**

   Click the resonance minimum on the curve to place marker `m1`, then double-click the graph (`✎ Edit`) → in the **Lines & Notes** tab, add a `-10 dB` horizontal pass line and press `m1 → note` to fix it as an arrow annotation.

3. **Show a secondary axis (Y2) at the same time**

   To overlay gain (`S21`, left axis) with return loss (`S11`) or phase (`∠S21`) in one figure, assign that curve to `Y2 (right axis)` in the **Traces** tab.

4. **High-resolution export**

   In the **Export** tab, save as lossless vector **SVG** for academic papers, **2× PNG** for presentation slides, or **CSV** for the numeric data.

17 CHAPTER

How to Read 3D E-Fields · H-Fields · Surface Currents and Far-Field Radiation Patterns Easily



If S-parameters are the report card that tells you "what score it got", 3D fields and radiation patterns are the X-ray photos that show "at which corner, and why, heat builds up, and where the waves leak". Master rainbow-color physics decoding and a 3-second antenna fault diagnosis.

You will learn

Decoding the physics of E-fields (E) · H-fields (H) · surface currents (Js) and Dead Copper miniaturization

Try it

The Directivity → Gain → Realized Gain 3-second fault-diagnosis funnel

Key concepts

The five key 2D/3D radiation-pattern metrics and re-solve-free beam steering with Edit Sources

17.1 Physics decoding table for 3D rainbow color maps: where should it be red?

When you turn on ribbon **Results ▶ Field Overlay / Field Slice**, **the physical meaning of red (maximum) and blue (minimum) is exactly opposite depending on which quantity you chose**! This one table lets you read every RF phenomenon right before your eyes.

Field type	Where red (the peak) appears	The practical judgment · prescription an engineer should make right away
E-field $\|\mathbf{E}\|$ [V/m]	Open ends where the voltage is maximum · **both ends of a patch · narrow coupling gaps**	① **The main culprit of dielectric heating** ($p_d \propto \omega\varepsilon''\|\mathbf{E}\|^2$) ② A **detuning-sensitive zone**, where the resonance shifts sharply when a finger or plastic case touches it ③ A high-power corona/arc-discharge risk point (prescription: corner fillets!).
H-field $\|\mathbf{H}\|$ · surface current $\|\mathbf{J}_s\|$	Shorting vias where current crowds · **patch center · inset neck · line edges**	① **The main culprit of copper resistive heating** ($p_c \propto R_s\|\mathbf{J}_s\|^2$; prescription: wider lines, parallel vias!) ② Cut a slot across the red current path, and the path detours, so **the effective length grows** (the principle of miniaturization!).
Blue zone (Dead Copper)	Outer corners of ground/pads where both $\|\mathbf{E}\|$ and $\|\mathbf{J}_s\|$ are blue	A **dead zone** that contributes almost nothing to radiation or matching! When you need to shrink the board, it's **the first place to cut away**, and a safe spot to drill mechanical mounting screw holes.

- `Chosen metals` **(scale for the chosen metals only)** — when one intense peak at the port feed makes the whole coupler or stub you actually want to see look solid blue, check only the traces you want to see, and the color map's maximum/minimum range is focused on those conductors.
- `Ex / Ey / Ez` **signed components & phase animation** — the magnitude (|**E**|) is always positive and shows only standing-wave nodes, but switch the component to `Ez` and play the phase ($0^\circ \rightarrow 360^\circ$), and **whether waves travel along the line and where the reflected standing waves sit** unfold like a movie!

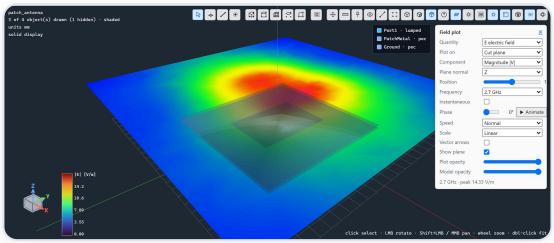


Figure 17-1 The |E| distribution on a patch antenna cross-section. You can see at a glance that strong fringing E-fields sit at both radiating edges, and that the very center of the patch is a voltage null (blue: a spot where a shorting pin can go!).

HOW TO **Zoom in on just the conductor current you want! 3D field slices & phase animation in 4 steps**

1. **Check Save fields**
   Check that the analysis finished with `Save fields` turned on at the frequency you want to view (e.g. 5.8 GHz) during the frequency sweep.
2. **Turn on surface current · cross-sections**
   In ribbon **Results ▸ Field Overlay**, choose the quantity `|Js| (Surface Current)`, or use **Field Slice** to turn on `|E|` on an `XY / XZ` cut plane inside the substrate.
3. **Optimize the scale**
   If fine patterns are hard to see, switch the color bar to **Log scale (dB)** and select only the traces of interest in `Chosen metals`.
4. **Track leakage with phase playback**
   Press animation ▶ **Play** and see with your own eyes whether the current flows to the intended output port or leaks into the bias line or a ground gap!

17.2 A 3-second fault-diagnosis funnel for the far field (Far Field): why is my antenna gain low?

The trap beginners fall into most often in antenna simulation is **confusing the three numbers Directivity, Gain and Realized Gain**! When the antenna gain comes out lower than expected, plug the three numbers into the **3-second diagnosis funnel** below, and you can tell on the spot whether the cause is the substrate material or the matching.

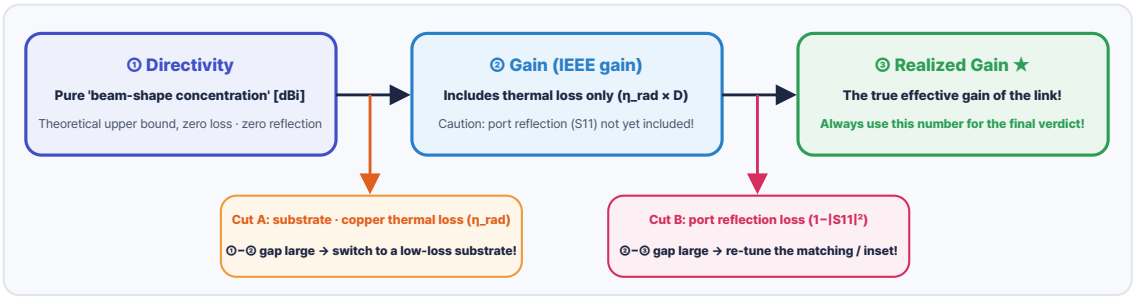


Figure 17-2 The physical relationship between the three far-field gain metrics, and the 3-second fault diagnosis. For the final communication-range calculation, always use Realized Gain, on the far right!

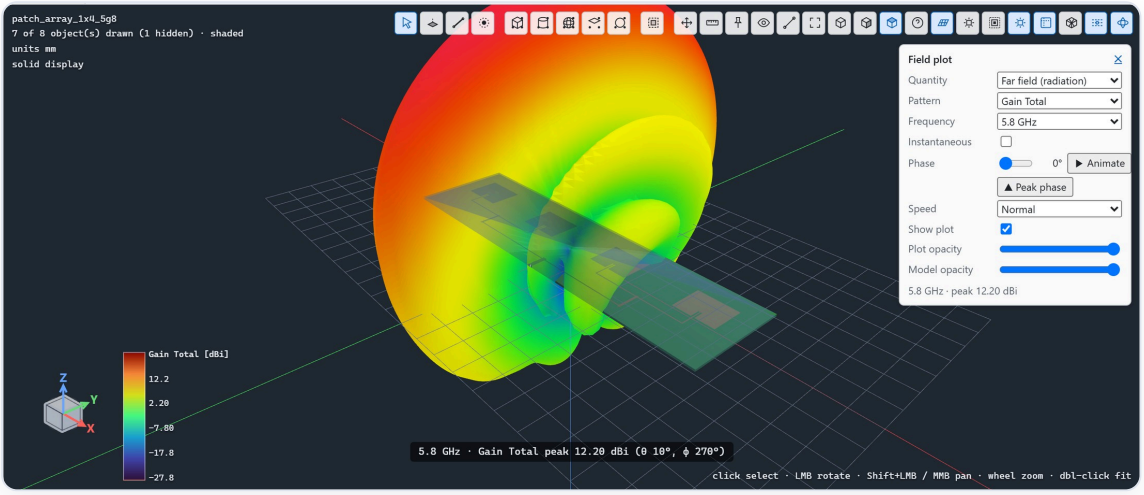


Figure 17-3 The 3D Realized Gain overlay of a 5.8 GHz 1×4 array antenna (peak 12.20 dBi). Make the substrate translucent with the Model opacity slider to see intuitively which way the beam points.

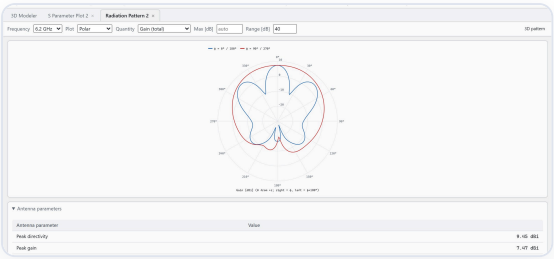


Figure 17-4 2D polar E-plane/H-plane cut patterns and the efficiency · beamwidth summary table below.

These are the **five key report-card numbers** to read from the 2D polar/rectangular radiation patterns (**Results ▶ Create Far-Field Report**) and the **Antenna Summary**.

- **Realized Gain [dBi]** — the effective amplification in the main-beam direction relative to an isotropic point source (0 dBi) (dipole about 2.15 dBi, single patch 5–7 dBi, 1×4 array 11–13 dBi).
- **Radiation efficiency η_{rad} [%]** — the fraction of the accepted power that flew off into space instead of burning up as heat (RO4003C patch 80–92 %, thick FR-4 patch 40–60 %).
- **Half-power beamwidth HPBW [°]** — the angular width between the two sides where it falls $-3\ \mathrm{dB}$ from the peak (narrower and sharper as you add array elements).
- **Sidelobe level SLL & front-to-back ratio F/B** — how far the largest sidelobe sticking out beside the main beam is suppressed (usually $\leq -13\ \mathrm{dB}$ recommended), and the back-leakage ratio ($\geq 15\ \mathrm{dB}$ recommended).
- **Axial Ratio [dB]** — the circularity report card of GPS · satellite circularly polarized antennas. If $\mathrm{AR} \leq 3\ \mathrm{dB}$ in the main-beam direction, the circular polarization passes!

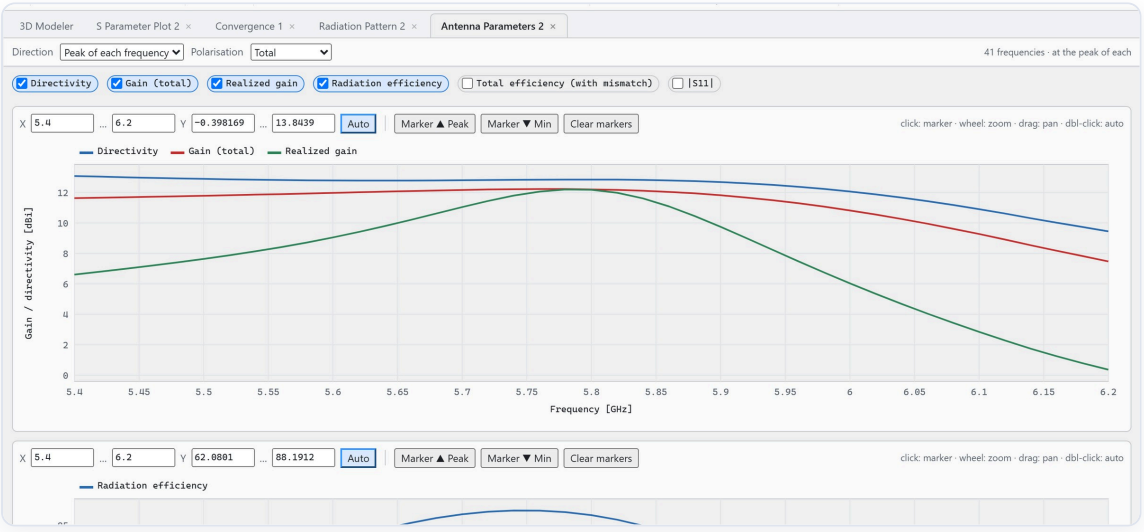


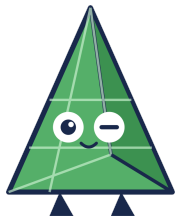
Figure 17-5 Directivity (blue), Gain (orange) and Realized Gain (green) compared at once versus frequency. At the 5.78 GHz match point, orange and green sit right on top of each other, but at both band edges you can clearly see how only Realized Gain plunges because of reflection loss!

17.3 Zero re-solve time! Real-time phased-array beam steering with `Edit Sources`

For a multiport array antenna, you only need to solve the 3D FEM once. Open **Simulation ▶ Edit Sources...**, enter evenly spaced phase differences for ports 1–4 (e.g. 0°, -45°, -90°, -135°) or Taylor amplitude weights, and the moment you press **Apply**, linear superposition of the EM fields updates **the 3D main-beam steering angle, sidelobe suppression and active reflection coefficient (Active S_{nn}) in real time, with zero re-solve time**.

18 CHAPTER

3-Line De-embedding · Vector Fit SPICE · Sharing with the 60 fps 3D Viewer



This chapter covers 3-Line De-embedding, which cleanly strips off port-launch parasitics with nothing but three lines of different lengths and no separate TRL calibration kit, passivity-corrected SPICE subcircuit extraction, and how to share results through the no-install 60 fps web 3D field viewer.

You will learn

Standard-free 3-Line port de-embedding and how to read Consistency

Try it

Passivity-enforced Vector Fit / SPICE (.sp) error checks

Key concepts

The standalone .html 3D viewer and automatic Korean/English PDF reports

18.1 Cutting out port-launch parasitics with `3-Line De-embedding` NEW V2.3 ONLY IN AETHER

Connector and Lumped Port feeds carry discontinuity parasitic inductance and capacitance (a "port edge error box") that blurs the S-parameters of the pure device (DUT). **Results ▸ 3-Line De-embedding...** mathematically back-solves and removes the error box **without Open/Short standards, using just three straight transmission lines (L_1, L_2, L_3) that share the same port launch and differ only in length**!

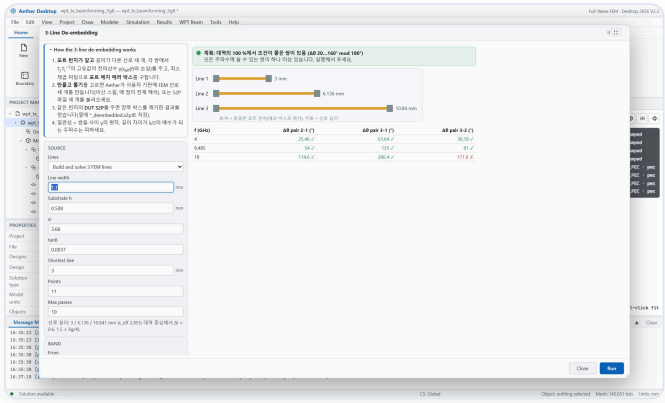


Figure 18-1 The 3-Line De-embedding dialog. Enter just the substrate data, and it automatically works out the three best line lengths that avoid half-wavelength (λg/2) singularities (e.g. 3 / 6.167 / 10.918 mm) and extracts the error box with a background FEM run.

- **The core equation** — from the eigenvalues of the cascaded transfer-matrix pair $T_j T_i^{-1}$, it extracts the pure line's complex propagation constant $\gamma(f) = \alpha(f) + j\beta(f)$ (the per-frequency $\varepsilon_{eff}(f)$ and $\mathrm{dB/mm}$ loss), independent of the port parasitics, then finds the left and right port edge error boxes (`*_errorbox.s2p`) by least squares and peels them off both ends of the DUT (`*_deembedded.s2p`).
- **File mode & automatic FEM mode** — you can load three `.s2p` files measured on real boards and use it for VNA measurement de-embedding, or let Aether create and solve the three lines automatically with `Build and solve 3 FEM lines`.

HOW TO **Strip port parasitics cleanly! Running 3-Line De-embedding & reading the Consistency result**

1. **Enter the band · substrate**
   Open **Results ▶ 3-Line De-embedding...** and check the band of interest (e.g. `1~20 GHz`) and the substrate thickness, permittivity and line width, and it automatically recommends three golden-ratio line lengths that avoid half-wavelength ($n\lambda_g/2$) singularities.

2. **Solve the 3 reference lines**
   Run **Build and solve 3 FEM lines** (or `Load .s2p files` if you have measured files) to extract the propagation constant $\gamma(f)$ and the port error boxes.

3. **Inspect the Consistency curve**
   Check that the `Consistency` **error curve** in the result window is low and smooth across the whole band (if a sharp spike rises at a particular frequency, the length difference ΔL has hit a multiple of a half wavelength, so recalculate with the recommended lengths).

4. **Save the DUT de-embedding**
   Specify your device's (DUT) S-parameters and press **De-embed DUT**, and you get a pure `*_deembedded.s2p` with the port-launch parasitics completely removed!

18.2 Straight to a time-domain circuit simulator: `Vector Fit / SPICE Macromodel` NEW V2.3

To feed frequency-domain S-parameters from 3D EM into an LTspice, Spectre or ADS transient (Transient) analysis, they must be converted into a rational-function pole-residue equivalent circuit.
Results ▶ Vector Fit / SPICE Macromodel... handles this in one click.

To prevent transient-analysis divergence (a numerical explosion in which energy is amplified without limit), always turn on the `Enforce passivity` **(passivity enforcement)** option. If the **RMS error** shown after fitting is `1e-3` (-60 dB) or less and the `Passive: YES` badge appears, you have a perfect SPICE `.subckt` netlist (`.sp`) that can't be told apart even when overlaid on the original EM curve.

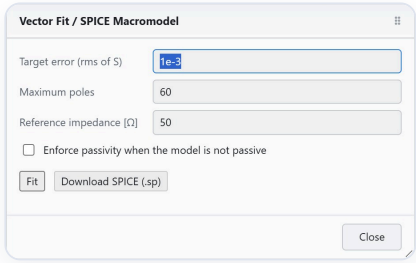


Figure 18-2 The Vector Fit / SPICE Macromodel dialog. It supports a target RMS error (1e-3), a maximum number of poles, and passivity enforcement.

18.3 Expression extraction (`Output Variables`) · automatic PDF reports · the 60 fps standalone `.html` viewer UPGRADE

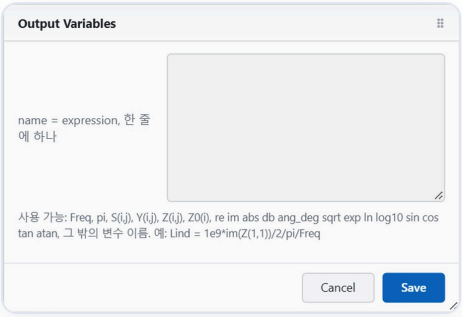


Figure 18-3 Output Variables. An expression such as im(Z(1,1))/(2*pi*Freq) instantly builds the effective L and Q curves of a spiral inductor.

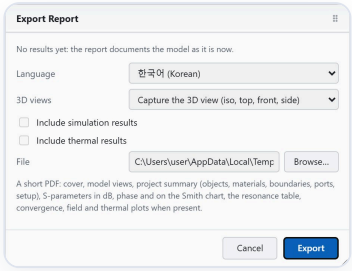


Figure 18-4 The automatic Korean/English PDF report generator. It bundles 4-direction 3D views, the setup summary, S-parameters, fields and even thermal results into one document.

The best way to send 3D fields to customers and colleagues who don't have the tool: the standalone `.html` 3D viewer

A single HTML file exported with **File ▶ Export ▶ ▶ Report (.html) / 3D Viewer** contains LP-quantized, compressed complex E-fields, H-fields, surface currents and 3D radiation patterns, together with the whole Three.js WebGL engine. The recipient needs neither Aether EM nor an internet connection: just double-click the file in Chrome or Edge to **rotate the drawing at 60 fps, slice it along any cut plane (Cut Plane), and operate the RF phase animation and port beam steering** themselves!

PART

05

Wizards & Automatic Design Encyclopedia From Spec Entry to Finished Antennas · PAs · Circuits · WPT

Microstrip matching that used to take a week of hand calculations and trial and error, 22 array antennas and metasurfaces, the 4-step GaN power amplifier (PA) chain, free-wiring schematic Co-sim, near-field focused wireless power (WPT) and cavity resonators — together with Wiz the wizard, we dig into the essence of practical automatic design: start in 1 second with formula synthesis (≈), and finish flawlessly with 3D Full-Wave FEM.



19 Wizard Ecosystem Map · Common UX · Transmission Line Wizard

20 Antennas in Two Stages: Antenna Wizard · Metasurface · Antenna Designer

21 Non-Orthogonal Automatic Routing (Smart Connect) and Array Feed Networks (Auto Feed)

22 The Three Manual Circuit-Synthesis Tools: Impedance Matching · Filter · Divider/Coupler

23 Power Amplifier (PA) 4-Step Mastery ①: PA Wizard & Bias Designer

24 Power Amplifier (PA) 4-Step Mastery ②: Class-F Auto-Stub & Real-Time PA Tuner

25 Nonlinear & Free-Wiring Schematic Co-sim (SPICE + EM + Back-Annotation)

26 Wireless Power Transfer · Beamforming · Cavity Resonance Workbench (WPT Beam)

19 CHAPTER

Wizard Ecosystem Map · Common UX · Transmission Line Wizard



Aether EM's wizards are not mere "calculators". They are intelligent design partners that read the project substrate on their own, diagnose physical limits and process tolerances with a 3-color traffic light, and carry you through 3D drawing generation and background FEM tuning in a single breath.

You will learn

The full wizard ecosystem map and the 4-step closed-loop philosophy

Try it

Automatic substrate recognition · 3-color traffic light · honest ≈ estimate marking

Key concepts

Transmission Line Wizard and the bench copper-tape back-solving recipe



Figure 19-1 A diorama of the wizard lab. From a few lines of spec, transmission lines, patch arrays, filters, power amplifiers and wireless-power beams rise up over a 3D board, and a converged 3D FEM always has the final say.

19.1 The Desktop 2026 V2.3 wizard ecosystem map at a glance

From a single passive component to multistage power amplifiers and wireless-power systems, pick the tool that fits your design task from the map below and jump right in. All the wizards are connected so they can pass data to one another.

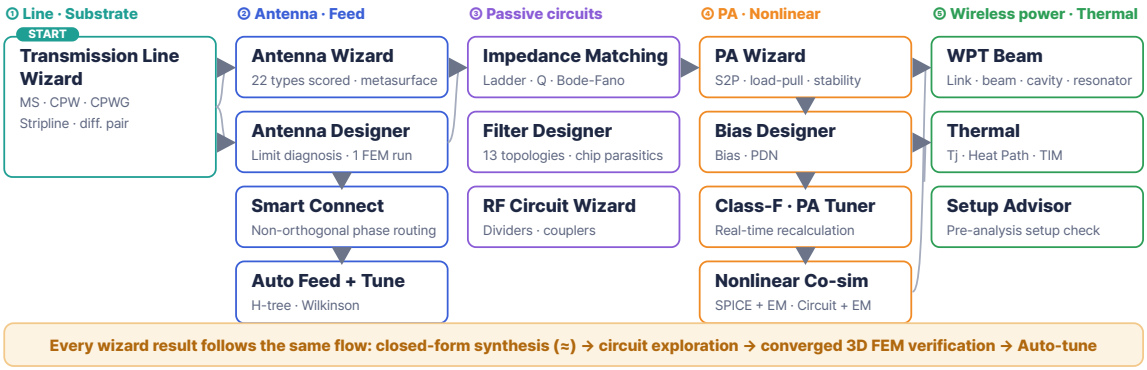


Figure 19-2 The full map of Aether EM's automatic design wizards. It flows organically from single-element synthesis to array feeding, the 4-step PA pipeline, schematic Co-sim and the WPT workbench.

19.2 The five golden UX rules every wizard shares, and engineering honesty

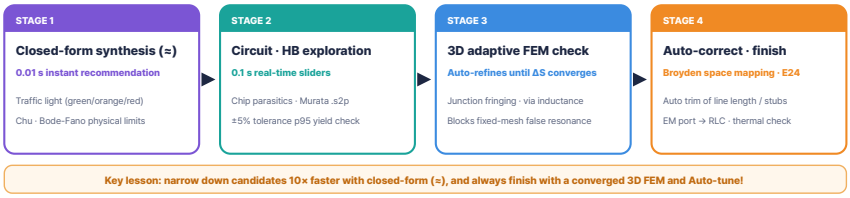


Figure 19-3 The common 4-step closed loop of the wizards: ① ultra-fast closed-form synthesis (≈) → ② circuit · tolerance exploration → ③ converged 3D FEM verification → ④ automatic dimension correction by space mapping / feedback.

1 · AUTO BOARD

Automatic project-substrate recognition

The moment the window opens, it finds the `Substrate` dielectric of the current design, fills in the material, thickness h, ε_r and $\tan\delta$ automatically, and shows a `✓ Board from the project` badge.

2 · MODELESS & FORMULA

Modeless 3D view & expression input

Freely rotate the 3D viewport behind the wizard window while it stays open, and type expressions and units such as `2*Wf` and `0.5mm+h` into any field (`Enter` recalculates, `Esc` closes).

3 · TRAFFIC LIGHT

The 3-color traffic light and one-line prescriptions

Green passes even with tolerance margin, **orange** passes only at nominal (with a prescription such as switching to a low-Q multistage design), and **red** warns of a Chu/Bode-Fano physical-limit violation or an unetchable feature (<0.1 mm).

4 · HONEST ≈ BADGE

Strict separation of estimates (≈) and real FEM results

Before you run 3D FEM, every number honestly declares with the `≈` **symbol** that it is a quasi-static formula estimate, and during a background analysis a ΔS **convergence mini sparkline** is shown live at the bottom.

19.3 The cornerstone of every RF design: `Transmission Line Wizard`

NEW V2.3

Draw ▸ Transmission Line Wizard... (ribbon **Home / Draw**) precisely synthesizes the frequency dispersion, loss and higher-order-mode limits of **5 transmission-line types**: microstrip, CPW, grounded coplanar (CPWG), stripline and differential coupled microstrip (Differential pair).

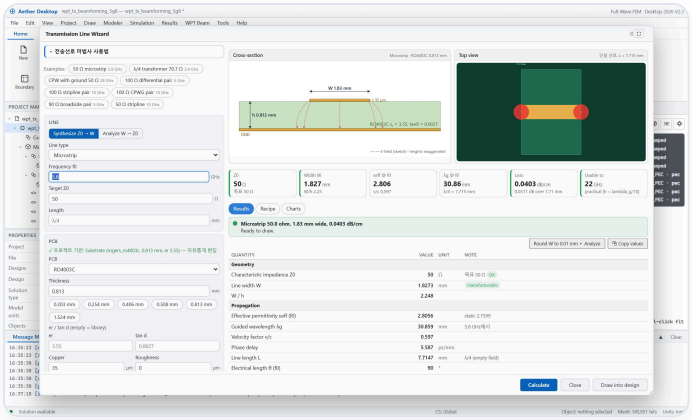


Figure 19-4 The Transmission Line Wizard. It automatically recognizes the project's RO4003C 0.813 mm substrate and instantly prepares the 5.8 GHz 50 Ω line width (1.83 mm) and 3D generation complete with ports and setup.

Why is it wrong to simply divide the length by 2 or 3 for harmonics?

As frequency rises, a microstrip's EM field is pulled further into the substrate, and the effective permittivity $\varepsilon_{eff}(f)$ grows: it undergoes **frequency dispersion (the Kirschning–Jansen / Frankel model)**. So the $\lambda_g/4$ length at $3f_0$ (17.4 GHz) is noticeably shorter than a simple 1/12 of the f_0 wavelength!

The wizard's `Result` tab gives, for each harmonic (f_0, $2f_0$, $3f_0$), an exact physical-length table calculated with the dispersive $\varepsilon_{eff}(nf_0)$ at that frequency, and also points out **the safe upper-limit frequency** f_{max} at which TE_1/TM_1 surface waves and transverse resonance begin.

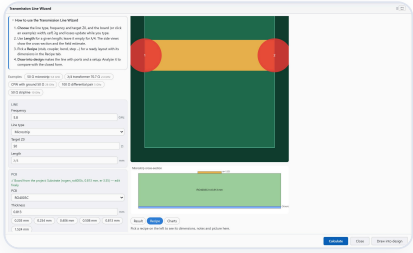


Figure 19-5 The Recipe tab, practitioners' favorite. Besides stub, taper and via-fence dimensions, it even back-solves the copper tape you stuck on during bench testing!



Wiz's auto-design recipe

ONLY IN AETHER Ever tuned a resonance in the lab by sticking a knife-trimmed piece of **copper tape** onto the end of a stub while watching the VNA? Enter the width × length in mm of the tape you stuck on in **Back-annotate measured tape** in the `Recipe` tab, found in no other commercial EM tool! It instantly back-solves the resonance shift (%) and the copper extension to apply in the next Gerber revision.

HOW TO **Generate a 50 Ω standard line in 3D, complete with ports and setup, in 30 seconds & read the dispersion results**

1. **Launch the wizard & check the substrate**
   Open **Draw ▸ Transmission Line Wizard...** and check that the `✓ Board from the project` badge (or the substrate preset you want) is selected at the top.

2. **Enter the line type · targets**
   Choose `Microstrip` or `CPWG` and enter `Frequency = 5.8 GHz`, `Target Z0 = 50 ohm`, `Electrical length = 90 deg`.

3. **Read the dispersion · mode ceiling (f_{max})**
   In the **Result** tab, check the calculated physical line width W, the loss per unit length (dB/mm), and that **the safe upper limit** f_{max}, where higher-order surface waves switch on, is comfortably above your highest operating frequency (if it's lower, switch to a thinner substrate!).

4. **One-click 3D assembly**
   Press **Build in 3D** at the bottom, and the substrate, ground, copper, input/output ports and analysis setup are all created at once, so you can go straight to `F9` verification.

20 CHAPTER

Antennas in Two Stages: Antenna Wizard · Metasurface · Antenna Designer



Learn the perfect teamwork of the Antenna Wizard, which explores the Pareto front of 22 antenna families and metasurfaces · FPRA from a system point of view, and the Antenna Designer, which takes a single antenna from its Chu physical limit through 30 % area miniaturization and automatic FEM tuning.

You will learn

Architecture selection (Antenna Wizard) vs precision synthesis (Antenna Designer)

Try it

The metasurface (Reflectarray) phase builder and FPRA resonators

Key concepts

The Chu–McLean physical limit · miniaturization trade-offs · 1-run FEM auto-tuning

20.1 Two antenna wizards: when should you open which?



Figure 20-1 Aether EM's two-track antenna design strategy. System exploration, arrays and metasurfaces are done in the Antenna Wizard; single-radiator limit checks, miniaturization and automatic FEM correction are done in the Antenna Designer.

20.2 Scoring 22 candidates and the Pareto front: `Antenna Wizard` + metasurface/FPRA NEW V2.3 ONLY IN AETHER

Enter the target frequency, bandwidth (%), required gain (dBi), allowed size and surroundings (free space, radome thickness · ε_r, metal-plate clearance, detuning near the human body) in **Draw ▸ Antenna Wizard...**, and it evaluates single and array configurations of **all 22 families (22/22 with full 3D generation!)** and ranks them on the Pareto front. In particular, when you pick an array candidate, it even routes a **coaxial-probe corporate feed network (Corporate Probe-Fed Array)** with phase imbalance within $< 0.5^\circ$ on the back substrate automatically, and right after creation a background FEM corrects the resonance scale factor (`k_len`) and the feed-position factor (`k_feed`) by itself!

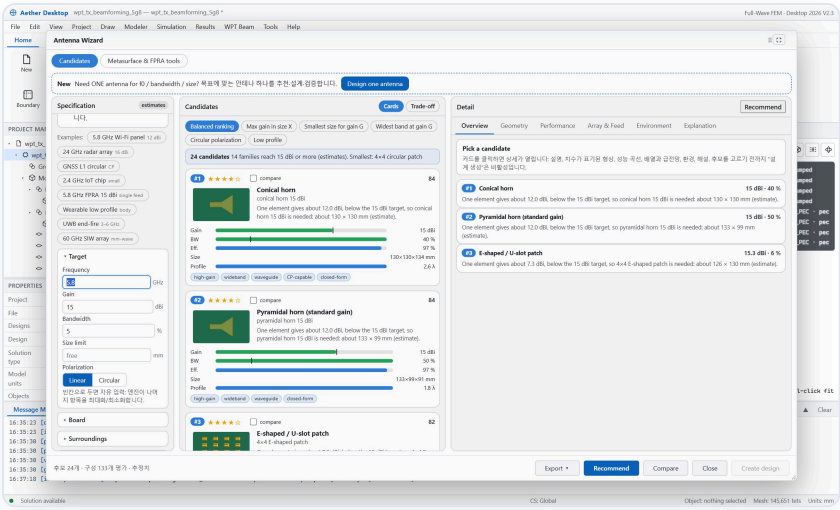


Figure 20-2 The 3-panel Antenna Wizard screen. For a 5.8 GHz 15 dBi target, it shows that a single patch can't do it, and automatically builds and compares a 4×4 E-slot patch, a dielectric resonator (DRA) and a stacked patch array.

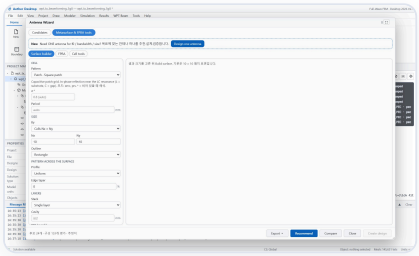


Figure 20-3 The Metasurface & FPRA tools mode at the top of the Antenna Wizard. It automatically synthesizes reflectarray/transmitarray phase layouts and the height of a Fabry-Perot resonator (PRS).

Reflectarray · metalens & FPRA designer (`Metasurface & FPRA tools`)

If you want 15–25 dBi of high gain from a single feed horn or one patch, press **Metasurface & FPRA tools** in the toggle at the top (this is an electromagnetic aperture synthesizer, not the general CAD face editing in `Faces`!).

- **Surface builder** — calculates the correction phase $\phi_{req}(x_i, y_j)$ each grid cell must produce for the feed position (x_f, y_f, z_f) and steering angle (θ_0, ϕ_0), places the whole 3D reflectarray/metasurface automatically with a unit-cell lookup table, and reports the quantization loss (dB) in advance.
- **FPRA (Fabry–Perot resonator antenna)** — from the reflection coefficient $|R|$, $\angle R$ of the partially reflecting surface (PRS), it finds the resonant cavity height $h \approx \frac{\lambda_0}{4\pi}(\angle R + \angle R_{\mathrm{GND}} + 2\pi N)$ and the directivity enhancement $\Delta D \approx \frac{1+|R|}{1-|R|}$, and creates the 3D structure immediately.

20.3 Precision synthesis of a single antenna and physical-limit diagnosis: `Antenna Designer` NEW V2.3

When you're taking one single antenna that fits your goal all the way to completion, open **Draw ▶ Antenna Designer...** (or the blue banner button at the top of the Antenna Wizard). For 16 antenna types, you step through the six tabs in order: **recommend → design → Chu physical limit → miniaturization → matching → FEM verification · auto-tuning**.

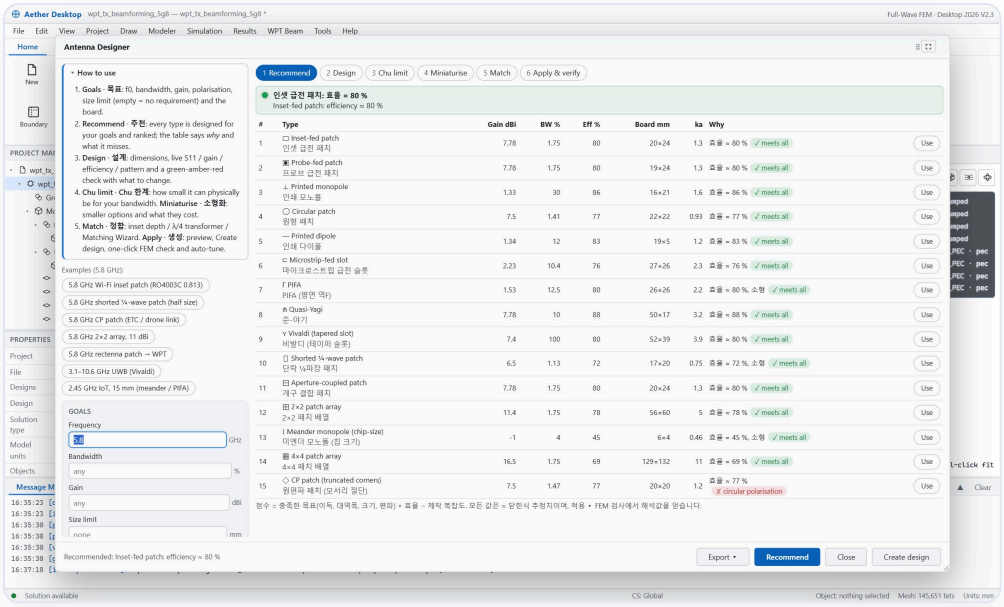


Figure 20-4 Step 1 of the Antenna Designer, the recommend tab. It synthesizes all 16 antenna types with real dimensions and compares gain, bandwidth, efficiency, enclosing-sphere size (ka) and the reasons they qualify at a glance.

Key physics ① — why can't a small antenna be both wideband and highly efficient? (`3 Chu limit`)

This is the tab that convinces people with the laws of physics instead of words, when you get an unreasonable mechanical request to fit a wideband, high-gain antenna into 10 mm! The minimum radiation quality factor Q_{Chu} and maximum 2:1 VSWR bandwidth of any linearly polarized antenna that fits inside a sphere of radius a are set by the Chu (1948)–McLean (1996) theorem.

$$Q_{\mathrm{Chu}} = \frac{1}{(ka)^3} + \frac{1}{ka}, \quad \mathrm{BW}_{\max,2:1} = \frac{1}{\sqrt{2}\,\eta_{\mathrm{rad}}\,Q_{\mathrm{Chu}}} \quad \left(k = \frac{2\pi}{\lambda_0}\right)$$



Wavy's EM principle note

Here is the decisive detail found only in the `Antenna Designer`! For a patch antenna, the ground plane acts as a mirror image, so the enclosing-sphere radius a is **taken from the size of the radiating patch**; but for **monopoles · PIFAs · meander antennas**, the current flowing on the ground plane is itself the main radiator, so **the diagonal of the whole board must be taken as** $2a$! If you enter an impossible spec, it back-solves the minimum enclosing-sphere diameter $2a_{min}$ exactly by bisection.

Key physics ② — what do you lose when you shrink the area to 30 %? (`4 Miniaturise` & `6 Auto-tune`)

Based on a 5.8 GHz RO4003C ($h = 0.813$ mm) inset patch, here is the practical report card per miniaturization technique compared in the `4 Miniaturise` tab, together with the 3D FEM auto-tuning results from the `6 Apply & verify` tab.

5.8 GHz antenna variant	Relative area	2:1 bandwidth	Predicted gain / efficiency	Initial FEM resonance → result after Auto-tune
Basic half-wave inset patch ($\varepsilon_r = 3.55$)	100 % (13.5×17.1 mm)	1.75 %	7.8 dBi / 80 %	5.905 GHz (+1.8 %) → **after 1 tuning run, 5.804 GHz,** $S_{11} = -23.8$ dB
Higher-permittivity substrate ($\varepsilon_r = 6.15$ / 10.2)	69 % / 51 %	1.25 % / 0.89 %	6.8 / 5.3 dBi	Trade-off: higher permittivity increases surface-wave loss and shrinks bandwidth
Shorted $\lambda/4$ patch (via-wall short)	Board 70 % (**patch 30 %**)	1.13 % (FEM 0.53 %)	6.5 dBi / 72 %	5.367 GHz (via L pulls it down) → **after 2 tuning runs, 5.799 GHz,** $S_{11} = -27.3$ dB
Chip-size meander monopole	**5 %** (6×4 mm)	4.0 %	−1.0 dBi / 45 %	For ultra-small IoT; more ohmic loss, and the pattern depends on ground-plane size

In addition, the `5 Match` tab shows the textbook inset-depth formula (cos^2) side by side with a practical EM-based empirical formula (cos^4) that corrects for the notch disturbance, and you can hand the finished antenna specs straight to the Ch. 26 wireless-power receiver with a single **Send to WPT RX** button.

HOW TO **A fail-proof antenna recipe, even for beginners: follow Antenna Designer tabs 1→6**

1. `1 Recommend` · **pick a candidate**
   Enter the target frequency, bandwidth, gain and maximum allowed size, then click the top antenna with a **green traffic light** in the table of 16 candidates.
2. `2 Design` · `3 Chu limit` **check**
   Check the automatically calculated initial dimensions, and in the **3 Chu limit** tab check that your antenna's point lies below the physical-limit curve (the feasible region).
3. `4 Miniaturise` · `5 Match` **settings**
   If the board area is too small, choose a $\lambda/4$ shorting via wall or a high-permittivity alternative in **4 Miniaturise**, and select the practical cos^4 inset feed (or a $\lambda/4$ transformer) in **5 Match**.
4. `6 Apply & verify` · **an automatic FEM bullseye!**
   Press the **Build 3D + Auto-tune (FEM)** button and wait a moment: the background 3D FEM corrects even the fringing error by itself and lands $S_{11} \leq -20$ dB right at the center of the target frequency!

21 CHAPTER

Non-Orthogonal Automatic Routing (Smart Connect) and Array Feed Networks (Auto Feed)



This chapter covers Smart Connect, which joins two lines at the electrical phase length you want without the reflections of right-angle bends, and Auto Feed Network, which automatically synthesizes and FEM-corrects a Wilkinson feed tree with precisely matched phase and amplitude once you click just 1 input and N outputs.

You will learn
Dubins shortest-path · phase-matched Smart Connect and Klopfenstein tapers

Try it
Auto Feed Network, done by selecting 1 common + N outputs

Key concepts
Feed Tune, cutting FEM phase error from 11.7° to 1.45°

21.1 Smooth phase routing with no right angles: `Smart Connect`

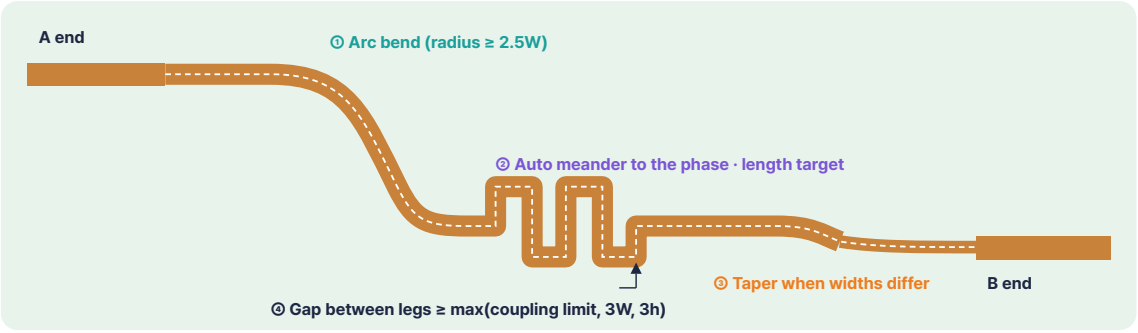


Figure 21-1 The 4 automatic synthesis elements of Smart Connect: arc/miter bends, a target-phase meander, a coupling-suppression gap, and an impedance taper.

In face-select (`F`) or edge-select (`E`) mode, `Ctrl`+click the ends of the two lines to connect, then press **Modeler ▸ Smart Connect ▸ ▸ Smart Connect...**

- **Auto (shortest Dubins path) · Phase (target phase θ) · Length (physical length)** — if the straight-line distance is shorter than the target phase calls for, it folds in a meander automatically with a safe gap that respects the coupling limit (default -25 dB, Garg–Bahl coupled-line model).
- **Automatic conversion between different line widths** — if the impedances at the two ends differ, it automatically inserts an equal-ripple, shortest-length **Klopfenstein taper** or a multistage binomial transformer.
- `Smart Connect Tune…` — measures the fine phase error caused by bends and coupling between adjacent legs from the real FEM S_{21} phase, and corrects it exactly within 1–3 runs.

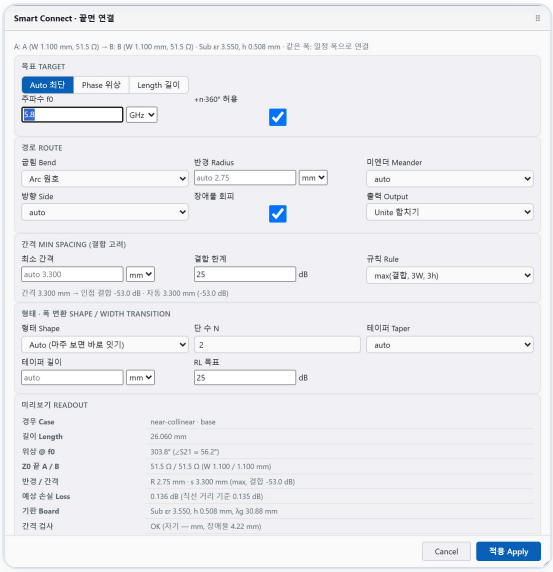


Figure 21-2 The Smart Connect live preview. It calculates a total length of 26.06 mm, a phase of 303.8° and a minimum coupling gap of 3.3 mm (−53 dB) before drawing anything.

21.2 Fully automating array feed trees: `Auto Feed Network` & `Feed Tune`

Drawing by hand a corporate distribution network that feeds a 4- or 8-element patch array with uniform excitation, low-sidelobe Taylor/Chebyshev tapers or beam-steering progressive phases ($0^\circ, 90^\circ, 180^\circ, 270^\circ$) takes two days. Now, **first click the common input end face, then `Ctrl`+click the output end faces in order**, and press ribbon **Draw ▸ Auto Feed Network** !

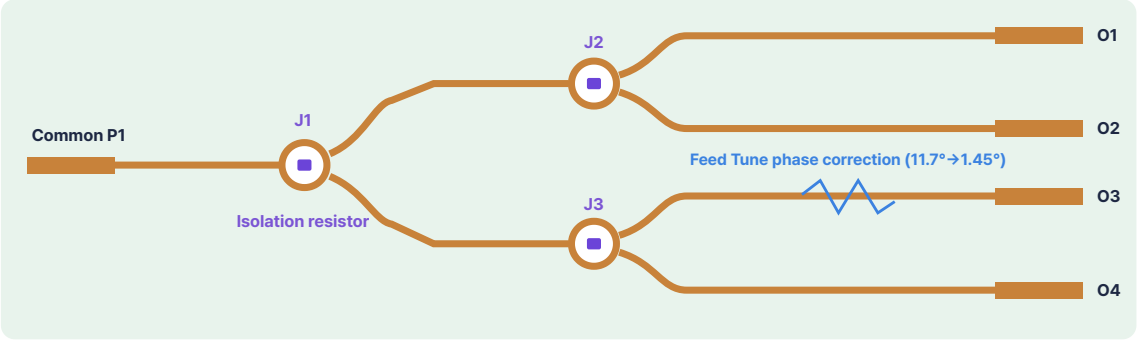


Figure 21-3 The automatically synthesized structure of a 1→4 feed tree. Depending on the available space, it places Wilkinson junctions (with RLC isolation resistors) or λ/4 T-junctions and inserts phase-correction meanders.

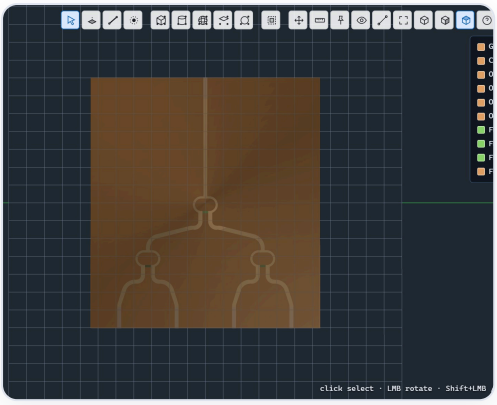


Figure 21-4 The synthesis result of a 5.8 GHz 1→4 Wilkinson feed tree, with tiny slivers healed automatically (heal_rings).

Feed Tune: fixing T-junction phase skew in a single run (`Feed Tune`)

When you first verify (`Verify`) in 3D FEM a 5.8 GHz $0/90/180/270^\circ$ progressive-phase 1:4 Wilkinson tree drawn from circuit formulas, the maximum phase error between outputs spreads to as much as 11.7° because of junction asymmetry and meander coupling.

Now press ribbon **Feed Tune** (**Auto Feed Network ▸ Verify / Tune...**) and run the correction loop **just once**: it feeds the phase and amplitude residuals measured in FEM back into each output's correction-line length and split ratio and re-synthesizes, converging in one go to production-grade performance with **a maximum phase error of** 1.45°**, an amplitude error of** $0.05\ \mathrm{dB}$ **and port isolation of** $19.1\ \mathrm{dB}$!

22 CHAPTER

The Three Manual Circuit-Synthesis Tools: Impedance Matching · Filter · Divider/Coupler



Pick a matching network that holds up even to ±5 % part tolerances on the dual Smith chart, draw filters with chip parasitics compensated in advance, and diagnose the temperature rise of a 500 W high-power coupler, and even isolation-resistor burnout in a fault.

You will learn
The dual Smith · rectifier diode · ferrite TLT matching wizard

Try it
Filter Designer with chip-parasitic pre-compensation (Compensate)

Key concepts
High-power stress diagnosis in the RF Circuit Wizard

22.1 `Impedance Matching Wizard` : taking responsibility for tolerances and parasitics NEW V2.3

Open **Draw ▶ Impedance Matching Wizard...**, and instead of blank fields, a practical example, **50 Ω → $10 + j20\ \Omega$ @ 5.8 GHz**, is synthesized instantly, showing left and right dual Smith charts and a ranked list of candidates.

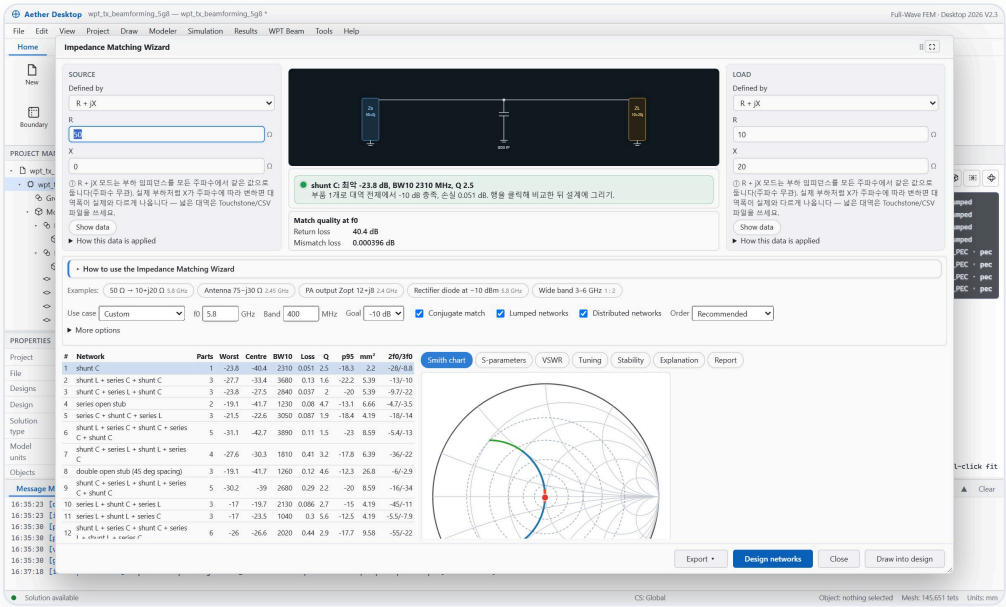


Figure 22-1 The Impedance Matching Wizard. Specify R+jX, Touchstone, the current EM result, a PA Zopt or a Schottky rectifier diode for the source (left) and the load (right) each, and compare the best matching networks.

- **The default part model is `Chip with parasitics`, not an ideal element!** — real 0402/0603 parasitic ESR and SRF (or the `Murata library`) are included by default, and the `p95` **column** of the ranked list shows the 95th-percentile worst-case $|S_{11}|$ from a Monte Carlo run on part values ±5%. A high-Q circuit that looks good only at nominal and falls apart at `p95` immediately gets an **orange traffic light**, along with a recommendation for a low-Q multistage L/Pi circuit.
- **Large-signal impedance of a rectifier diode (`Diode at Pin`) & back-off check** — enter Schottky diode parameters for a WPT rectenna and the input power P_{in}, and it automatically extracts the large-signal input impedance, checks at the same time that the match doesn't collapse even at 10 dB lower power, and passes it straight on with **Send to Co-sim**.
- **VHF/UHF wideband `TLT / ferrite`** — below a few hundred MHz, when a $\lambda/4$ line would be larger than the board, it proposes coaxial Guanella/Ruthroff transmission-line transformers (TLT) and even checks for ferrite-core flux saturation (B_{max}).

22.2 `Filter Designer`: pulling in ahead of time the cutoff that chip parasitics would shift UPGRADE

Draw ▶ Filter Designer... synthesizes 13 LPF · HPF · BPF · BSF topologies as microstrip patterns, chip RLC ladders, or hybrids (printed L + chip C).

The highlight is the **parasitic compensation (Compensate)** option! It back-calculates in advance how far the cutoff frequency will sag because of SMD pad parasitic capacitance, via inductance and the chips' own ESL, **pre-distorts the prototype element values so that the response hits the target exactly once the parasitics are added**, and then snaps them to E24 standard values. After drawing, use **Results ▶ Compare with Circuit Model...** to compare three curves on one chart: ideal circuit, circuit with parasitics, and real 3D FEM.



Figure 22-2 The Filter Designer dialog. Remember that the fc of a Chebyshev filter is the ripple-edge frequency, not the −3 dB point!

22.3 `RF Circuit Wizard`: checking high-power heating and dielectric breakdown too UPGRADE



Figure 22-3 The RF Circuit Wizard. It recommends 10 divider · coupler · hybrid topologies and supports Draw & Tune automatic correction.

It synthesizes 10 types on the substrate: Wilkinson, the high-power grounded-resistor **Gysel**, Branch-line, the wideband interdigital **Lange**, the Rat-race 180° hybrid and multistage binomial transformers. In particular, enter the input power `Pin [W]` (e.g. a 433 MHz 500 W coupler), and it diagnoses in advance **the trace temperature rise ΔT, the insulation margin for the peak RF voltage, and the power dumped into the isolation resistor if an antenna line breaks (P_{fault})**, preventing resistor burnout accidents.

HOW TO **Reading the matching and filter wizards' result tables properly, and verifying with a 3-curve comparison**

1. **Read the p95 tolerance column, not the nominal**
   In the `Impedance Matching Wizard` ranked list, don't be dazzled by the nominal $|S_{11}|$ number: choose a low-Q circuit whose `p95` **column**, the worst case under ±5% part error, is -10 dB **or below (green light)**.

2. **Turn on parasitic pre-compensation (Compensate)**
   In `Filter Designer`, check **Compensate** to pre-compensate how far pad and via parasitics will push the cutoff, then run **Build in 3D** and the `F9` analysis.

3. **Compare 3 curves: circuit vs 3D EM**
   Open **Results ▸ Compare with Circuit Model...** from the top menu and check that the three curves, **ideal circuit (dashed) · circuit with parasitics · real 3D FEM (solid)**, overlap in the passband and the stopband slope!

23 CHAPTER

Power Amplifier (PA) 4-Step Mastery ①: PA Wizard & Bias Designer



The two real reasons high-power GaN PA designs so often fail, "out-of-band low-frequency gate oscillation at 350 MHz" and "bias isolation ruined by via inductance", are brought fully under control with the two wizards in the first half of Aether's PA pipeline!

You will learn

Aether's integrated 4-step PA pipeline

Try it

The 17-device PA chip library · load-pull · competing external schematics

Key concepts

PDN anti-resonance damping · via-parasitic lessons (55→18.2 dB) · removing 350 MHz oscillation

23.1 Aether EM's 4-step PA design pipeline



Figure 23-1 The integrated 4-step power-amplifier design chain: ① PA Wizard basic matching · stabilization → ② Bias Designer PDN · bias tee → ③ Class-F intrinsic-drain harmonic shaping → ④ PA Tuner 0.1 s real-time trimmers and integrated thermal verification.

23.2 Step 1 — `PA Wizard` and the 17 verified devices in the `PA Library`

NEW V2.3

Draw ▶ PA Wizard... and **Tools ▶ PA Library...** come with 17 representative RF power devices with cited datasheet sources, including MACOM/Wolfspeed (`CGH40010`, `CG2H40010`, `CG2H40120`), Ampleon (`BLF188XR` 1.4 kW LDMOS), Analog Devices and Mini-Circuits, and you can load your own `.s2p`, load-pull (`.lp` / `.csv`) and datasheet impedance tables directly.

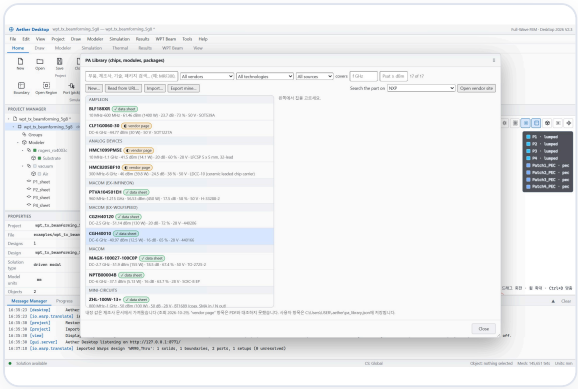


Figure 23-2 The PA Wizard. From the device S2P and load-pull data, it derives stabilization circuits, a ranking of input/output matching pairs and predicted large-signal curves in one go.

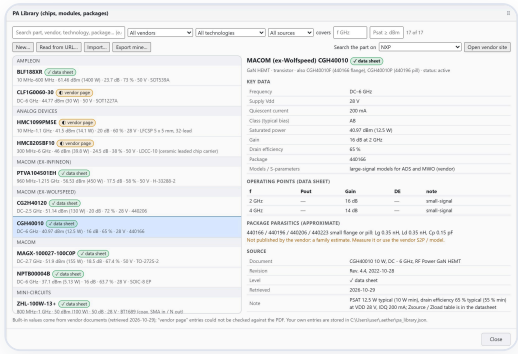


Figure 23-3 The PA Library (17 built in + user extensions). Search operating band, saturated output, efficiency and package thermal resistance Rjc at a glance.

- **Import competing external KiCad / ADS / AWR / Qucs / SPICE schematics** ONLY IN AETHER — if you already have matching circuits laid out in KiCad (`.kicad_sch`), ADS, AWR, Qucs or a SPICE netlist (`.net`), load them as they are and pit their gain, ripple and stability head-to-head, in the same ring, against the candidates the wizard synthesized automatically!
- **Full-band stability (K, $\mu > 1$) and automatic stabilizing resistors** — it detects potential oscillation regions where the geometric stability factor $\mu < 1$ not only at the operating frequency but across the whole low-frequency band, and adds a gate series/parallel RC stabilization network in one click. (Note: the large-signal curves inside the PA Wizard are estimates based on the small-signal S2P + load-pull Z_{opt} + a Rapp saturation model.)

23.3 Step 2 — `Bias Network Designer` : catching hidden oscillation and memory effects NEW V2.3

Think a bias circuit is "just a thin $\lambda/4$ line with a capacitor on it, done", and you'll get burned! **Draw ▶ Bias Network Designer...** designs not only RF isolation but also **the 1 kHz ~ 20 GHz power distribution network (PDN) impedance** and low-frequency loop stability at the same time.

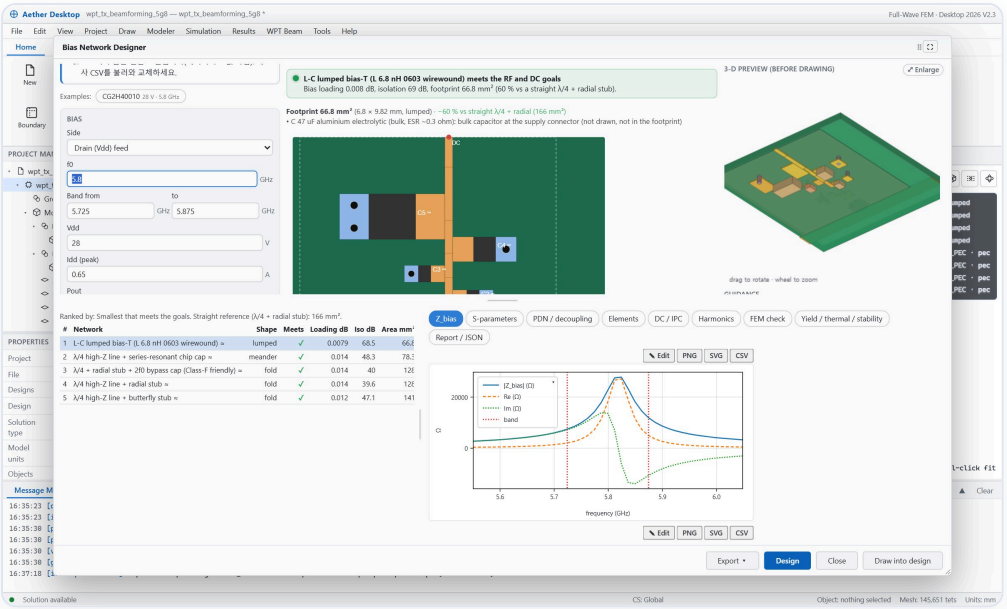


Figure 23-4 The Bias Network Designer. For a CG2H40010 5.8 GHz drain bias, it automatically compares and 3D-previews a 66.8 mm² lumped L-C bias tee, 60 % smaller than a straight λ/4 + radial stub (166 mm²), along with folded meander candidates.

CREW COMIC **Three practical lessons in bias design — the traps that catch you if you trust only the circuit simulator!**

Porty Huh?! In the ideal circuit, a single 0402 bypass cap gave **55 dB** of isolation at 5.8 GHz, so why does it crash to **18.2 dB** when I run 3D FEM, with RF power leaking straight into the supply?

Wavy Because the parasitic inductance of the pad and the two ground vias (hundreds of pH) stands there as a series reactance at 5.8 GHz! On the other hand, use a radial stub + `FEM stub trim` (1.03× correction), and you easily get **45.2 dB of isolation** even in real 3D FEM!

Wiz What's more, put a lossless L-C choke on the gate side and a $|\Gamma_S\Gamma_{in}| > 1$ **low-frequency oscillation around 350 MHz** easily breaks out. The gate current is almost zero, so choose the **gate-resistor feed (`r_feed`, 220 Ω)** topology and the full-band oscillation vanishes like magic!

- **Detecting PDN parallel anti-resonance ringing & the damping resistor R_{damp}** — when the ESL of a 100 pF RF cap and the capacitance of 10 nF/1 µF bulk caps create a parallel anti-resonance peak at tens of MHz, the envelope of modulated signals gets distorted (memory effect). The `PDN / decoupling` tab calculates the **video bandwidth** that keeps $|Z_{\text{PDN}}| < 0.1R_{\text{opt}}$, and proposes an exact $R_{\text{damp}} \approx \sqrt{(L/C)}$ only in the low-frequency stage, where it doesn't touch RF loss.
- `Send to Class-F (2f0 short)` — hands the baton straight to the next-step Class-F tool, so that the $\lambda/4$ bias line doubles as the $2f_0$ even-harmonic short-circuit stub!

24 CHAPTER

Power Amplifier (PA) 4-Step Mastery ②: Class-F Auto-Stub & Real-Time PA Tuner



The highlight of PA design: set the 2f0 short and 3f0 open at the true "current-source plane inside the die" hidden behind the package parasitics, shrink the area by 55 %, and then tune the input/output trimmers and even the heat sink in 0.1 seconds on top of the 4-port EM result!

You will learn
Intrinsic drain current-source de-embedding and 55 % miniaturization

Try it
Automatic convergence by Broyden space mapping (EM tune)

Key concepts
The 0.1 s real-time PA Tuner and the lesson of fundamental–harmonic interaction

24.1 Step 3 — why does the textbook $\lambda/4$ stub fail on a real GaN package? (`Class-F Auto-Stub`) NEW V2.3 ONLY IN AETHER

The heart of a high-efficiency Class-F amplifier is shaping the drain voltage waveform into a square wave to eliminate the loss area where it overlaps the current; in other words, **making the $2f_0$ even harmonic a short ($\Gamma = -1, 180^\circ$) and the $3f_0$ odd harmonic an open ($\Gamma = +1, 0^\circ$)**. But put a textbook $\lambda_g/4$ stub on the microstrip right outside the package lead, and the efficiency actually plunges! Why?

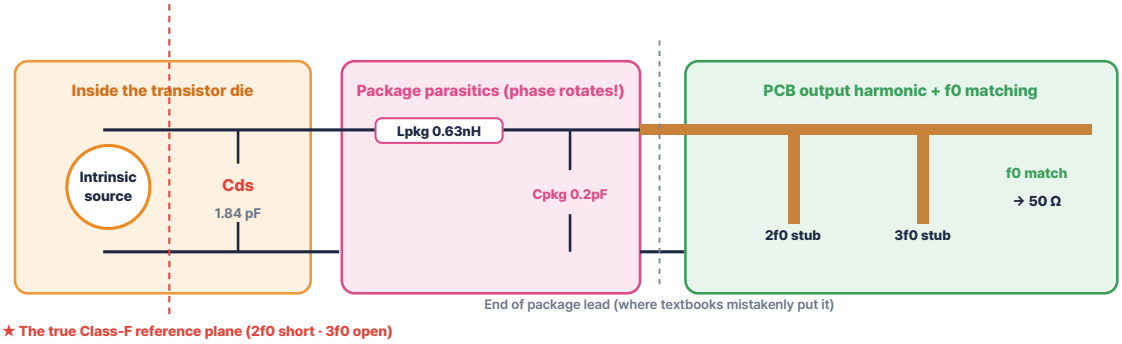


Figure 24-1 The intrinsic drain current-source plane (Intrinsic Plane) vs the package lead plane. Passing through the bondwire Lpkg (0.629 nH) and the drain-source capacitance Cds (1.84 pF), the 2f0 · 3f0 target phases you have to create outside the package rotate to completely different angles!

For example, at 5.8 GHz the $C_{ds} = 1.84$ pF of the CG2H40010 is already only $-j5\ \Omega$ at $3f_0$ (17.4 GHz), and the L_{pkg}–C_{ds} series resonance sits at 4.68 GHz. So when you select the output line and run **Modeler ▶ RF ▶ Class F on Output Line...**, the tool de-embeds the package parasitics, **plots on the Smith chart the harmonic reflection phases the current source inside the die really wants**, and shows as the top metric **the drain harmonic-balance efficiency (DE %)** solved over the full $f_0 \sim 7f_0$ network (if the stub position is off by just 1.5 mm, the harmonic score collapses from $0.78 \rightarrow 0.17$!).

MINIATURISE −55%

55 % less area at the same efficiency

Searches for $\lambda_g/2$-periodic solutions within 0.2 %p efficiency loss and gathers the stubs on one side of the line, shrinking the output section by up to 55 % (980 → 659 mm^2 achieved on the CG2H40010 board).

SMITH DRAG & MC

Smith drag & 400-board tolerance

Drag the $2f_0/3f_0$ markers on the Smith chart with the mouse and the stub lengths and positions are back-calculated live; a 400-run Monte Carlo checks the efficiency spread under ±0.05 mm etching error.

BROYDEN EM TUNE

Automatic output space-mapping tuning

`Extract EM stub model` extracts the T-junction fringing extension (+0.48 mm), and Broyden Jacobian space mapping (`EM tune`) converges the correction within 2–3 FEM runs.

24.2 Step 4 — zero re-solve, done with sliders: the real-time `PA Tuner`

NEW V2.3 ONLY IN AETHER

Run a precise EM analysis of the passive board **just once** as 4 ports (`RF_In` , `Gate` , `Drain` , `RF_Out`), and the magic begins the moment you set the `Result set` on the left to the `PA Tuner (live, editable)` tuner in **Results ▶ PA Results** (ribbon **Home ▶ PA Results**)! The series/shunt trimmer 2-port ladders (T_{trim}) attached to each port are not approximations: they are coupled to the 4×4 board matrix in 0.01 s by an exact closed-form port-extension formula (`extend_port` : $S_{\text{ext}} = S_{aa} + S_{ap}\Gamma_{\text{net}}(I - S_{pp}\Gamma_{\text{net}})^{-1}S_{pa}$).

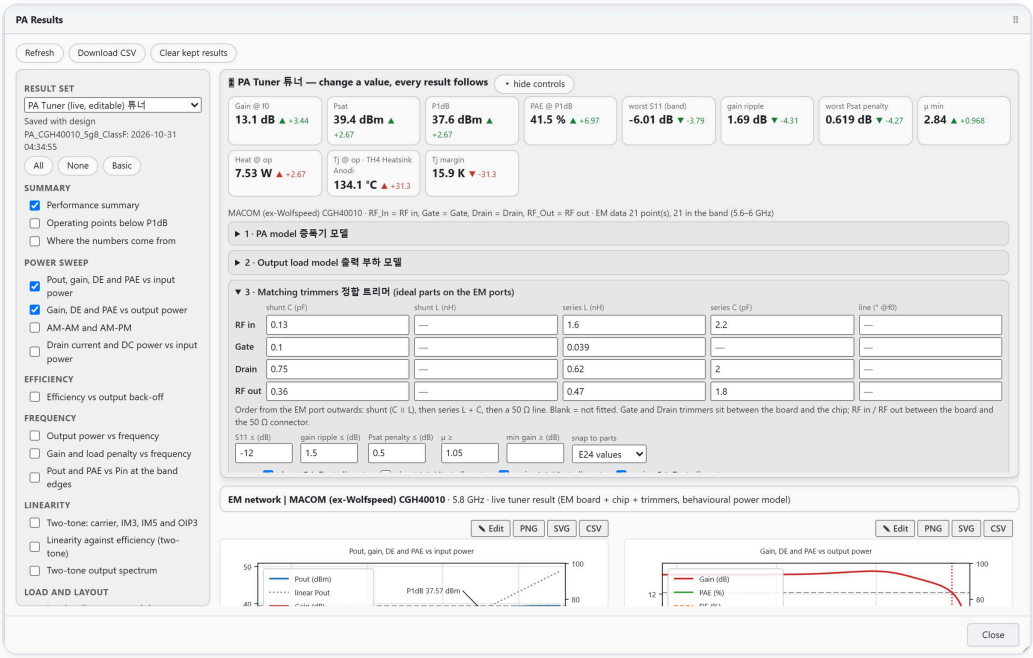


Figure 24-2 The real-time PA Tuner dashboard (CGH40010 5.8 GHz). Change the input/output 4-port trimmer L/C values or press Auto-tune (E24 snap), and within 0.1 s the gain (13.1 dB), Psat (39.4 dBm), PAE (41.5 %), stability (μ=2.84), anodized heat-sink junction temperature (Tj=134.1 °C) and 30 charts all update at once!

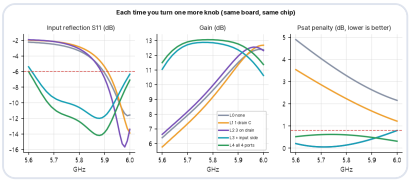


Figure 24-3 How S11 (−2.2 → −6.0 dB) and in-band gain (ripple 6.0 → 1.69 dB) recover as the trimmers are switched on from L0 (bare board) to L4 (all 4 ports, E24-snapped).

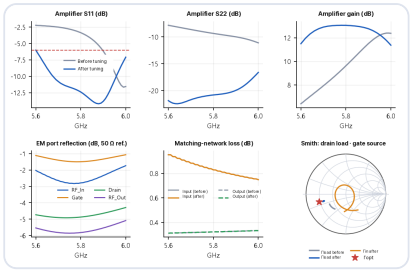


Figure 24-4 Stripping the mismatch reflection mixed into plain |S21| to isolate, as $-10\log_{10}(\mathrm{MAG})$, the pure substrate copper · dielectric dissipation loss (0.2–0.4 dB).

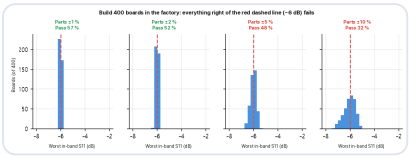


Figure 24-5 A 400-board dice experiment with ±5 % part tolerance: tune right onto the target (−6.0 dB), at −6.01 dB, and factory yield drops to a coin-flip 48.5 %!

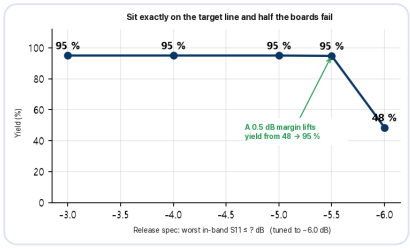


Figure 24-6 The production expert's +0.5 dB margin rule: tighten the Auto-tune target by just 0.5 dB to −6.5 dB and run it again, and the ±5 % yield jumps straight to 95 %!

- **A real recovery case (CGH40010 v2)** — for the bare board's mismatch revealed by converged FEM ($S_{11} = -2.22$ dB, in-band ripple 6.00 dB), running the PA Tuner's `Auto-tune` (global differential evolution → Nelder-Mead → exhaustive snap to E24 standard part values) brought it back to life in just a few seconds without re-meshing: worst in-band S_{11} -6.01 dB (-12.40 dB at the 5.8 GHz center), gain ripple 1.69 dB, and a P_{sat} load penalty of 0.62 dB (you'll practice this yourself in the Ch. 36 mission!).
- **The MAG metric, which isolates pure dissipation loss** ONLY IN AETHER — in an impedance-transforming network ($50\ \Omega \to Z_{\mathrm{opt}}$), the 50 Ω-referenced $|S_{21}|$ is full of mismatch reflection, so it's easy to mistake the board for having large heat loss. The PA Tuner precisely separates out only the pure copper · dielectric heat loss using $-10\ \log_{10}(\mathrm{MAG})$, based on termination-independent maximum available gain.

A must-read lesson for advanced designers (CGH40010 v3): the clash between the fundamental shunt C and the harmonic stubs!

If you first put a large shunt capacitor for fundamental matching (e.g. 2.04 pF, $-j4.5\ \Omega$ at 17.4 GHz) right in front of the drain, it shorts $3f_0$ by itself and disables the $3f_0$ open stub behind it. Also, **if you turn the drain trimmer far in the PA Tuner with no harmonic constraint, the board's carefully set $2f_0$ short phase ($-172^\circ \to +109^\circ$) can be thrown off**. So for high-efficiency Class-F designs, always align the harmonics and the fundamental together on the board with the integrated fundamental re-matching loop of `Class-F Auto-Stub`, and use the PA Tuner for fine connector trimming and yield · thermal verification!

24.3 The KPI report card at the top of `PA Results`, read at a glance & production pass criteria

When you first open the `PA Results` window, which of all those numbers and charts should you look at first? Just check the 7 summary cards at the top against the criteria below, and the amplifier's health is clear in 10 seconds!

Key result metric (KPI)	Practical production pass line	Interpreting a failure & the immediate prescription
`μ min` **(minimum stability)**	**Full band** ≥ 1.05**, mandatory!**	Below 1.0 is the #1 oscillation risk! Add a gate series R-C or a resistive bias feed (220 Ω).
`worst S11 (band)`	Standalone ≤ -10 dB (before an isolator ≤ -6.5 dB)	The input Smith chart (blue trace) strays from the center → input 2-port trimmer `Auto-tune` (+0.5 dB margin).
`Gain @ f0` & `Gain ripple`	In-band ripple $\leq 1.5 \sim 2.0$ dB	Large ripple means the match has collapsed at one band edge → stagger the input and output resonances slightly toward the top and bottom of the band.
`worst Psat penalty`	$\leq 0.6 \sim 0.8$ dB	The orange load trace on the output Smith chart has been pushed outside the red Z_{opt} contours → correct the drain matching line width and length.
`PAE @ P1dB / Psat`	Class AB 40–55 % / Class F 55–70 %+	If `DE` is high but only `PAE` is low, blame **insufficient gain** or output-board copper loss (check `-10 log MAG`!).
`Tj @ op` & `Tj margin`	**Margin** $\geq +15$ K (no runaway)	If a red warning appears, cut R_{ca} with black anodizing on the heat sink ($\varepsilon = 0.85$) or a copper coin/cut-out jig (Ch. 31).

25 CHAPTER

Nonlinear & Free-Wiring Schematic Co-sim (SPICE + EM + Back-Annotation)



Learn Nonlinear Co-sim, which dissects the power budget and reverse-voltage breakdown (−BV) of Schottky rectifier diodes precisely with harmonic balance, and schematic Co-sim, which plugs chip parts tuned on a free-wiring SVG canvas back into the 3D EM model.

You will learn

Schottky rectifier harmonic balance (K≥8) and the Rectifier Report

Try it

Free-wiring SVG schematic Co-sim and Bayesian PCE optimization

Key concepts

The Apply ▼ → EM port → Lumped RLC finalize back-injection loop

25.1 Dissecting Schottky rectifiers and their power budget: `Nonlinear Co-sim` & `Rectifier Report`

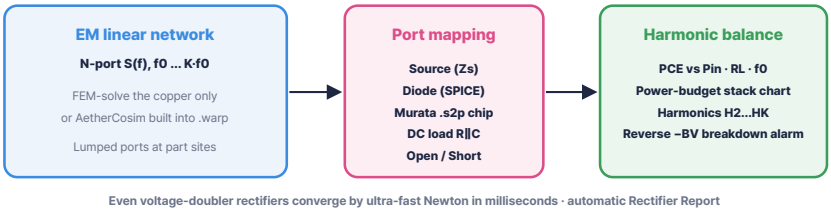


Figure 25-1 Passive patterns are solved once in EM with just their ports opened, and the nonlinear Schottky diodes and load are coupled by frequency-domain harmonic balance (HB).

For circuits with diodes, like a 5.8 GHz rectenna, set a wide EM sweep range **from 0.5 GHz or lower (for DC extrapolation) up to the highest harmonic** Kf_0 (e.g. 24 GHz for $K = 4$; $K = 8$ is recommended for high precision — **a small** K **overestimates efficiency by 3–4 %p!**), solve it once, and then run **Results ▶ Nonlinear Co-sim (SPICE + EM)...** and **Results ▶ Rectifier Report...**.

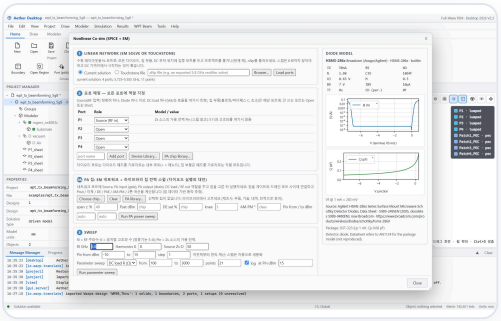


Figure 25-2 The Nonlinear Co-sim window. It includes the I-V/C-V curves and package parasitics (Lp, Cp) of built-in, datasheet-verified diodes (HSMS-282x/285x/286x, SMS7630, NT9000–9003).

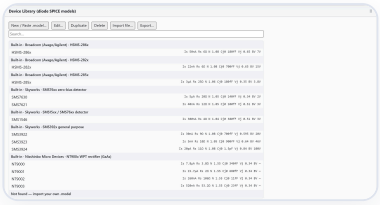


Figure 25-3 The Device Library. It holds only official datasheet SPICE parameters, and you can freely add your own .model/.lib files.

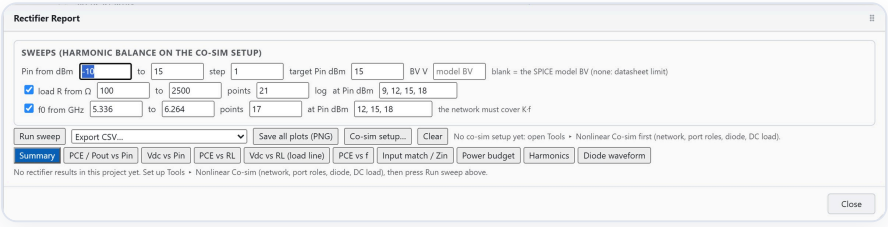


Figure 25-4 The Rectifier Report integrated sweep window. It automatically runs a triple sweep of input power (Pin), load resistance (RL) and frequency (f0), and extracts the power-loss breakdown (reflection vs substrate loss vs diode Rs loss) and reverse-breakdown (near −BV) warnings in one go.

CHART 1 · POWER BUDGET

How to read the cumulative power-loss bars

The input 100 % is split by color into reflection loss · EM substrate loss · diode R_s loss · harvested DC power (PCE). A large reflection bar calls for the matching network; a large diode bar calls for switching to a low-R_s device!

CHART 2 · PCE VS PIN & −BV

Reading the cliff and breakdown on the input-power curve

The low-power climb is the threshold-voltage (V_{bi}) region and the peak is the optimum; if efficiency drops sharply at high power, the time waveform $v_j(t)$ has hit the red reverse-breakdown line (`-BV`) (switch to a high-voltage device or a voltage doubler!).

25.2 The magic of the free-wiring SVG canvas and 3D back-annotation: `Co-sim (Circuit + EM)` NEW V2.3 ONLY IN AETHER

When you want to draw circuits freely, beyond fixed forms, open **Results ▶ Co-sim (Circuit + EM)...** from the top menu (window title: **Schematic Co-sim**)! Next to the current design's multiport EM block (updated automatically by fingerprint comparison on re-analysis!), wire up with the mouse ideal elements, parts with parasitics (`CREAL/LREAL`), 54 Murata `.s2p` **chips (** `CHIP` **)**, microstrip (`MLIN`), Schottky diodes (**200× faster than before**, using a current-residual Newton solver for voltage-doubler rectifiers!) and PA chips.

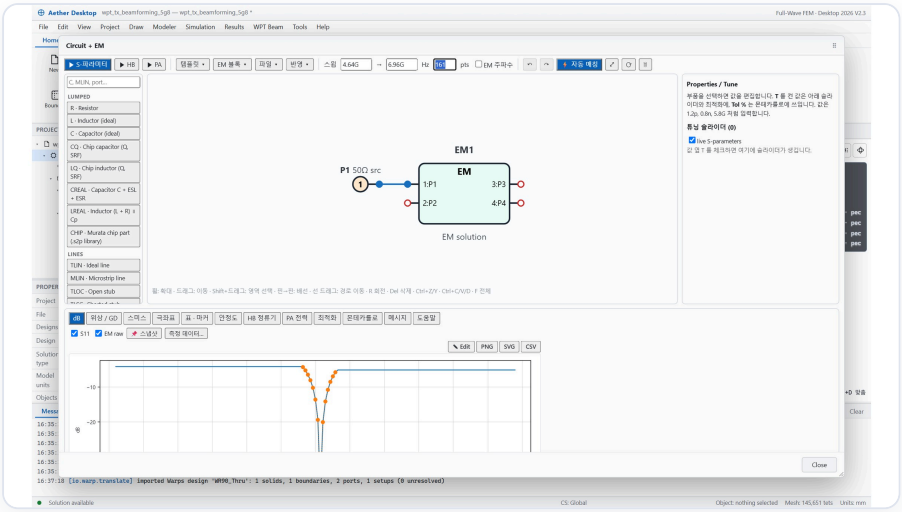


Figure 25-5 The schematic Co-sim (Circuit + EM) editor: wiring an NT9001 diode pair and L/C parts with parasitics to a 7-port rectifier EM block (S7P), and tuning S11 and HB rectifier efficiency at the same time with the live sliders on the right.



Figure 25-6 The schematic Co-sim → 3D EM Lumped RLC back-annotation (Back-Annotation) finishing flow that cuts practical design time to a tenth.

BEST PRACTICE **Pad-gap ports → 1-second schematic tuning → finalize as 3D EM Lumped RLC!**

1. **Open Lumped Ports in the pad gaps**
   Attach a 50 Ω Lumped Port at every SMD part pad site on the 3D board and run FEM **just once**.

2. **Schematic Co-sim sliders & Bayesian optimization**
   In the schematic editor, push the sliders, or use the `Optimize` tab (Bayesian TPE supported — **you can even maximize the rectifier's HB conversion efficiency PCE % directly!**), E24 snapping and the `Monte Carlo` yield curve to settle the best part values in seconds.

3. **One-click back-annotation to the 3D model!**
   Press **Apply ▼ ▶ EM port → Lumped RLC finalize** on the top toolbar, and the R/L/C and chip values you just found are replaced in bulk with **real Lumped RLC boundaries** at the matching Lumped Port positions in the 3D model (full Undo support). Finally, run `F9` just one more time for the final sign-off, including 3D coupling between parts!

26 CHAPTER

Wireless Power Transfer · Beamforming · Cavity Resonance Workbench (WPT Beam)



When does near-field spherical-wave focused beamforming work a +17 dB miracle, and when does it stop at +0.3 dB? Why does the human safety limit (10 W/m²) pin a ceiling on received power regardless of transmit power? Master all the physics of WPT, right up to 91.9 %-efficient 433 MHz resonant charging inside a metal chamber.

You will learn

Spherical-wave integration · Goubau efficiency · the truth about focusing and Fresnel number (NF≥1)

Try it

Retrodirective pilot tracking (+6 dB) and the 10 W/m² safety-ceiling law

Key concepts

Automatic 433 MHz Cavity WPT design and the mandatory 34.2 kV/m interlock

26.1 The three physical regimes of wireless power, and the dedicated `WPT Beam` workbench NEW V2.3

The ribbon **WPT Beam** tab and the top **WPT Beam** menu calculate the link budget precisely, even at close range where the far-field approximation (Friis formula) breaks down, using **an exact 3D spherical-wave distance R_{mn} integration over every transmit–receive element pair** and the Goubau wave parameter $\tau = \frac{\sqrt{(A_t A_r)}}{\lambda d}$ ($\mathrm{BCE}_{\max} = 1 - e^{-\tau^2}$).

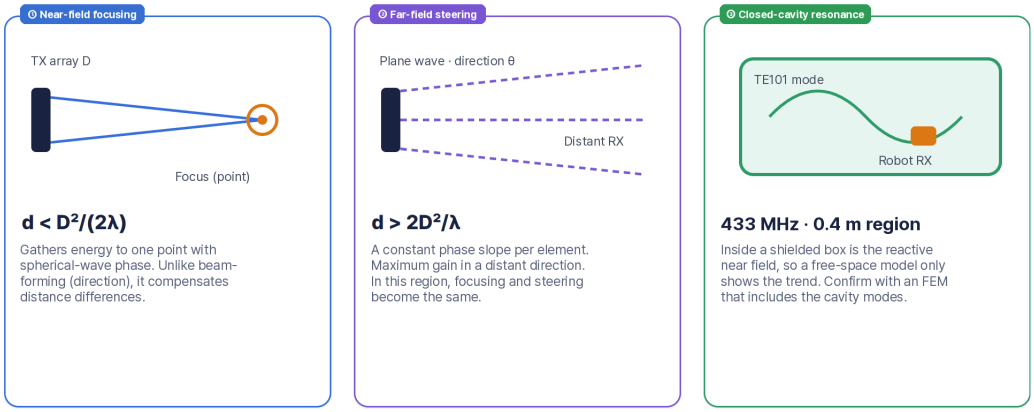


Figure 26-1 A physical comparison of radiative near-field focusing (NF ≥ 1) vs far-field steering vs closed-cavity resonance (Cavity WPT), and the human-exposure safety limits.

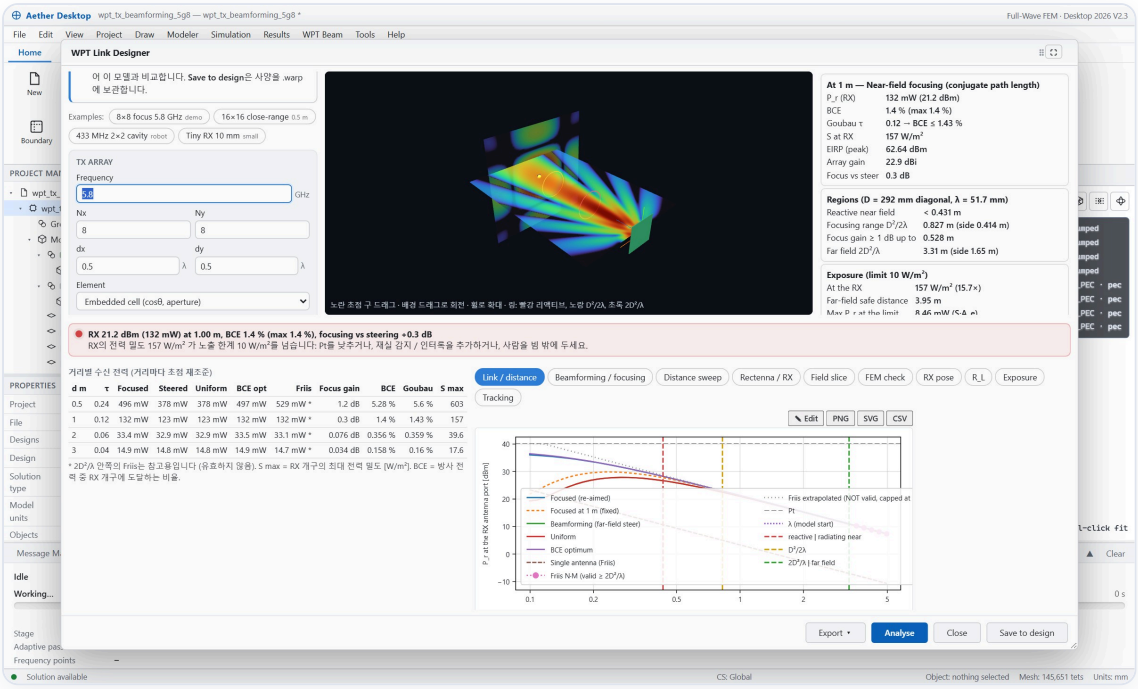


Figure 26-2 The WPT Link Designer (5.8 GHz 8×8 demo). It diagnoses on one screen the 3D beam cross-section slice, Focused/Steered/Goubau/Friis comparison curves versus distance, and the warning when the 10 W/m² human-exposure limit is exceeded.

26.2 Three decisive truths about beam WPT every practitioner must know

TRUTH 1 · FRESNEL

Near-field focusing works only at $N_F \geq 1$!

If the Fresnel number $N_F = \frac{(D/2)^2}{\lambda d} < 1$, the $1/R$ decay overpowers the phase reinforcement and the peak is pulled forward (**focal shift**). Fire 1 m at 5.8 GHz with an 8 × 8 array ($D = 292\ \mathrm{mm}$), and $N_F = 0.21$, so the focusing gain is only **+0.3 dB**; but fire 0.5 m with **16 × 16 ($D = 585\ \mathrm{mm}$), and a whopping +17 dB (410 mW vs 7.8 mW)** bursts out!

TRUTH 2 · SAFETY CAP

The human safety line ($10\ \mathrm{W/m^2}$) pins the maximum power

The MSIT · FCC · ICNIRP general-public exposure limit is $S_{\lim} = 10\ \mathrm{W/m^2}$ ($1\ \mathrm{mW/cm^2}$). In any space people can enter, no matter how high you raise the transmit power, **the maximum received power is fixed at $P_{r,\max} \approx S_{\lim} A_{e,\mathrm{RX}} \cdot \mathrm{PCE}$!** To deliver more, widen the receive aperture A_e or an unmanned interlock is mandatory.

TRUTH 3 · RETRODIRECTIVE

For moving targets, retrodirective pilot tracking is the answer

The retrodirective (Retrodirective) method, which fires back the conjugate ($-\angle V_{\mathrm{pilot}}$) of the pilot phase sent by the receiver, loses only 0.015 dB to 6-bit phase-shifter quantization, and in the `Tracking · figure-8` motion simulation it records **21.4 mW (+5.99 dB)** versus a fixed beam (5.16 mW)!

In addition, **RX position · pose** in the ribbon `Safety · Motion` group quantitatively breaks down offset, tilt and polarization-rotation loss ($cos^2\psi$), and the **human-exposure map** calculates in one click the keep-out zone (Keep-out zone) radius, local SAR from the Gabriel skin model, and the maximum transmit-power back-off that complies with legal limits.

26.3 The ultimate answer for shielded boxes and robot charging:

`Cavity WPT Designer` **NEW V2.3** **ONLY IN AETHER**

When charging robots and sensors moving inside a metal storage box or an industrial shielded chamber, **WPT Beam ▶ Cavity / Box WPT...** (ribbon **Cavity resonator 433 MHz / 2.4 GHz**), which uses the whole chamber as a high-Q resonator instead of a free-space beam, delivers overwhelming efficiency.

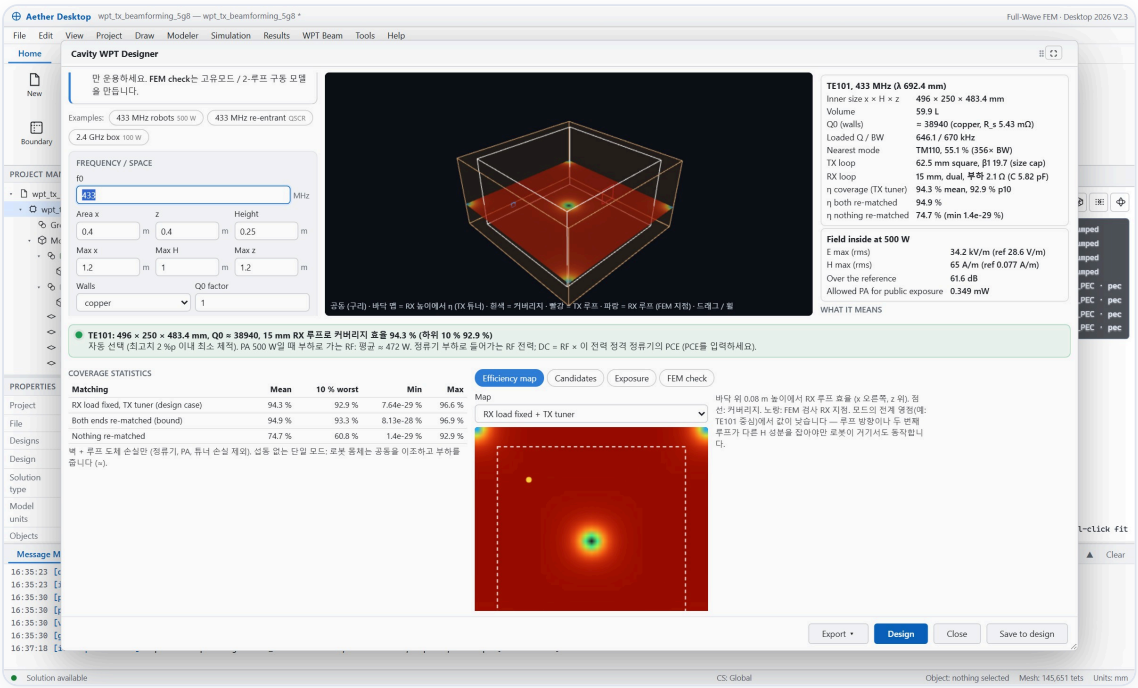


Figure 26-3 The Cavity WPT Designer (433 MHz robot, 500 W example). It automatically synthesizes a minimum-volume TE101 copper chamber (496×250×483.4 mm, Q0 ≈ 38,940) that pushes neighboring parasitic modes beyond 3·BW, plus a tiny 15 mm receive loop, achieving an average efficiency of 94.3 % (91.9 % verified by 3D FEM) over 90 % of the floor area!

Two iron rules of Cavity WPT physics and safety: magnetic-field nulls and the 34.2 kV/m high-voltage interlock!

- **Watch out for mode standing-wave nodes (Magnetic Null)** — like the green dots on the efficiency map at the bottom of the figure above, if a single loop sits on a flux node such as the center of TE_{101}, or the loop plane lies parallel to the flux, coupling drops to zero. For moving robots, always use **dual orthogonal loops** or dual-mode excitation.
- **Absolutely sealed shielding & a door interlock are mandatory!** — put 500 W into a chamber with an unloaded $Q_0 \approx 38{,}940$, and the internal peak E-field reaches a staggering $34.2\ \mathrm{kV/m}$ **(+61.6 dB over the general-public exposure limit!)**. It must never operate with a person inside or the door open, and **fully sealed metal walls plus a dual hardware interlock that cuts RF power the instant the door opens** are mandatory.

HOW TO **Judge the received wireless-power mW and the legal human safety distance in 3 minutes**

1. **Open the link designer**
   Open ribbon **WPT Beam ▶ WPT Link Designer** and enter the operating frequency (e.g. `5.8 GHz`), transmit and receive aperture sizes, transfer distance d and transmit power.

2. **Read the Fresnel number (N_F) & the 4 curves**
   Check that the Fresnel number at the top is $N_F \geq 1$ (below 1, the focusing gain is negligible!), then compare the received power of **Focused (near-field focusing)** · **Steered (plane wave)** · **Goubau (physical upper bound)** · **Friis** on the distance graph.

3. **Check the human-exposure safety line**
   Click the ribbon **human-exposure map** to see the **red keep-out radius (Keep-out zone)** where the $10\ \mathrm{W/m^2}$ legal limit is exceeded, and in an occupied space back off to at or below the indicated safe transmit power!

PART

06

Thermal Workbench & Cooling Design From Junction Temperature Tj to Black Anodizing and Thermal-Runaway Prevention



However perfect the S-parameters are, once the GaN transistor's junction temperature Tj passes 150 °C, efficiency falls off and thermal runaway burns the device out! In Part 6, together with Thermy the cooling coach, we master — in plain terms — everything from the physics of the independent thermal workbench that does not disturb the EM model by even a single bit (|ΔS| = 0.0), through node-split TIM, thermal-via · copper-coin · PCM helpers and Temp→RF two-way back-coupling, to the black-anodized heatsink and metal jig design that lower the temperature by 26 K without a fan.

27 Intro to the Thermal Workbench: EM Integrity (|ΔS|=0) and First Steps in Heat-Transfer Physics

28 The Three Heat Sources, Node-Split TIM and the Magic of Thin Copper

29 Practical Guide to the Five Cooling Helpers: Thermal Via · Copper Coin · Spreader · PCM · Pulse

30 Thermal-Bottleneck Tracing (Heat Path) · Auto-Optimization · Temperature → RF Two-Way Coupling

31 [Special Feature] Integrated Electro-Thermal Cooling Design of a GaN PA and the Metal Jig

27 CHAPTER

Intro to the Thermal Workbench: EM Integrity (|ΔS|=0) and First Steps in Heat-Transfer Physics



Grasp conduction · convection · radiation heat transfer clearly through the "voltage · current · resistor · capacitor" analogies most familiar to electromagnetic (EM) engineers, and learn the structure of the thermal workbench that finishes in 5 steps without touching your existing EM results at all.

You will learn

The independent AetherThermal structure that guarantees EM integrity (ΔS=0)

Try it

Thermal resistance Rth and thermal time constant τ, understood through the electric-circuit analogy

Key concepts

Convection-coefficient h chips and nonlinear Stefan–Boltzmann radiation physics

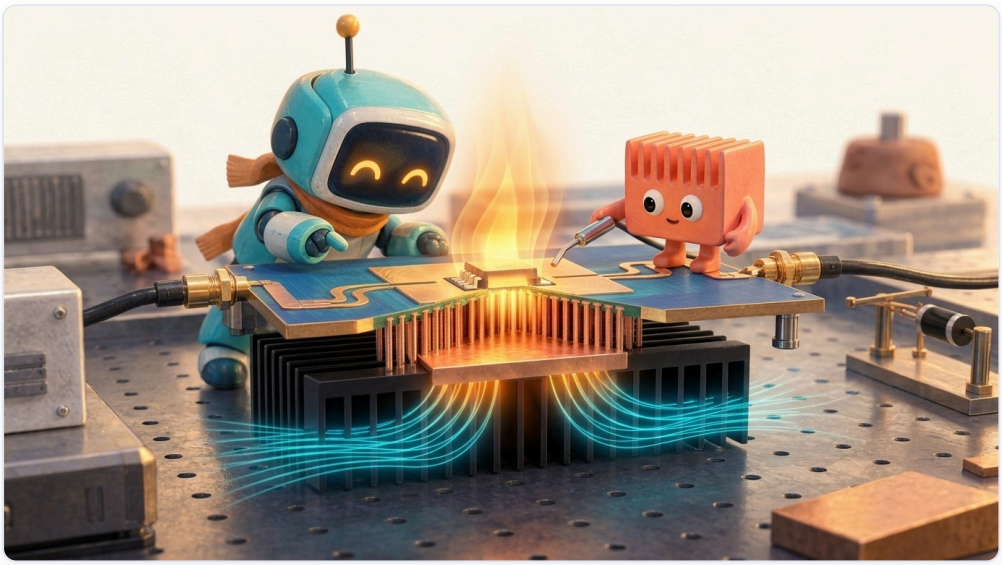


Figure 27-1 A thermal-lab diorama. The whole journey — heat from the transistor die spreading through the solder (TIM), copper coin and thermal vias to the black-anodized cooling fins, and escaping by convection and infrared radiation — is tracked with 3D FEM.

27.1 Why can EM engineers use it right away, without a separate CFD tool?

Traditionally, to see the temperature of an RF board you had to export the CAD and rebuild the boundaries and mesh from scratch in a separate mechanical thermal-analysis program. Conversely, you might also worry that touching thermal settings in the same file would break the S-parameters you had worked so hard to converge. Aether EM's **Thermal Workbench** solves both concerns at once.

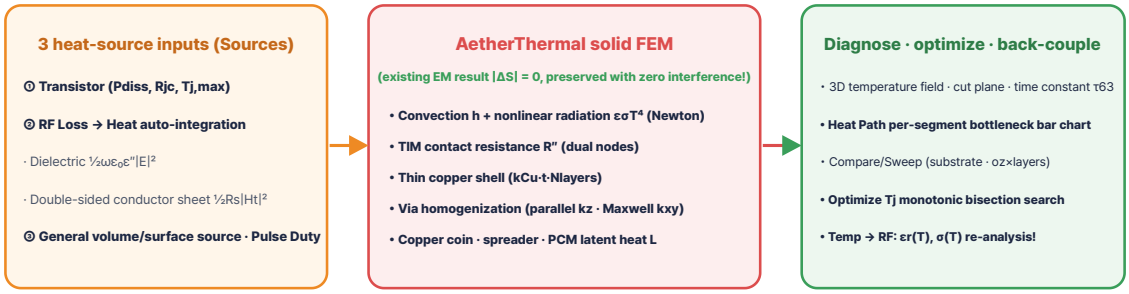


Figure 27-2 The Thermal Workbench architecture, running on the same 3D drawing in complete isolation from the EM domain, and its two-way coupling loop.

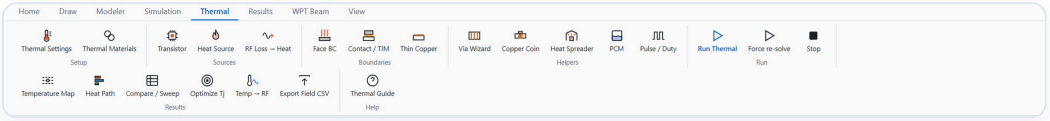


Figure 27-3 The dedicated Thermal ribbon tab. From left to right, it flows Setup → Sources → Boundaries (boundaries · TIM · thin copper) → Helpers (the 5 cooling helpers) → Run → Results (bottleneck · optimization · Temp→RF).



Figure 27-4 Click the Thermal tab and the left tree switches instantly to the dedicated thermal-workbench tree (go back and forth to the EM tree any time with the Model Tree link).

Thorough EM-integrity guarantee: `|ΔS| = 0.0`

ONLY IN AETHER

All thermal properties · heat sources · convection · TIM settings are written only to the independent `AetherThermal` block inside the `.warp` file, and the outermost air box (`Air`) is automatically excluded from the thermal model. Across all 8 shipped verification examples (Th1–Th8), the EM S-parameter difference before and after the thermal settings was verified to be exactly $|\Delta S| = 0.0$! (It is intentionally reflected in the EM only when you insert a new real 3D metal shape, such as a copper coin, or apply hot materials with `Temp → RF` .)

27.2 3-minute heat-transfer physics for RF engineers: it's exactly Ohm's law!

If thermal analysis is unfamiliar, remember just the one table below. **The heat-transfer equation is a 1:1 mathematical twin of a DC electric circuit!**

Electric-circuit concept	Heat-transfer counterpart	Key formula · physical intuition
Current I [A]	Heat flow Q [W]	The flow of heat energy per second poured out by the transistor or line losses.
Voltage drop ΔV [V]	Temperature rise ΔT [K or °C]	The temperature step created each time heat passes through a resistance (a 1 K difference = a 1 °C difference).
Resistance $R = \frac{L}{\sigma A}$ [Ω]	**Conduction resistance $R_{\text{cond}} = \frac{L}{kA}$ [K/W]**	Heat escapes better the thinner the thickness L, and the larger the thermal conductivity k (copper 401 vs FR-4 0.3!) and cross-section A.
Termination resistor	**Convection · radiation resistance $R_{\text{conv}} = \frac{1}{hA}$**	Widen the surface area A (heatsink fins!) and raise the airflow (h) and surface emissivity (ε) for heat to leave well into the air.
Capacitor C [F]	**Heat capacity $C_{\text{th}} = \rho c_p V$ [J/K]**	It can't change the steady-state temperature, but it slows the temperature spike during a pulse burst (time constant $\tau = R_{\text{th}} C_{\text{th}}$).

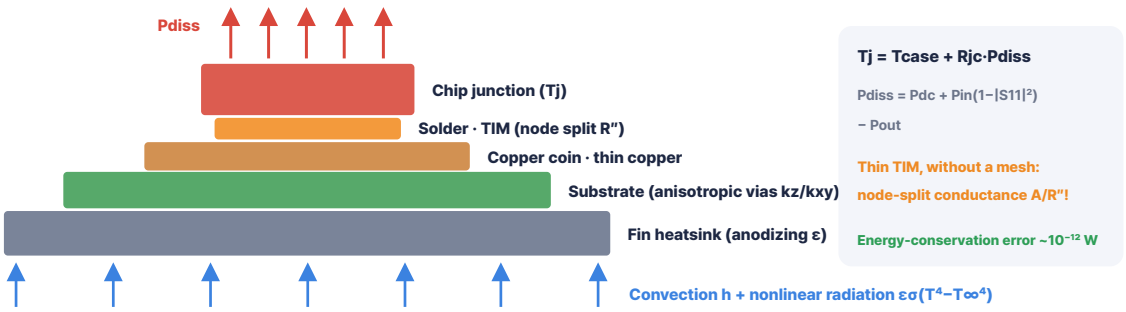


Figure 27-5 The series-parallel thermal-resistance ladder running from the chip junction (Tj) to the ambient air (T∞). You have to break through the single segment with the highest resistance (the bottleneck) to bring the temperature down.

27.3 Key settings in `Thermal Settings` and `Thermal Materials`

In **Thermal Settings** you set the ambient temperature T_∞, convection coefficient h and default emissivity ε applied by default to unassigned outer faces, and whether to run a steady-state or transient analysis.

- **One-click convection h chips** $[W/(m^2 \cdot K)]$ — sealed natural convection `5` · open still air `10` · small fan `30` · forced air `100` · liquid cold plate `1000`.
- **Automatic 5τ transient integration** — if you leave the transient end time at `0`, the solver estimates the model's thermal time constant τ on its own and **calculates automatically up to about 5τ**, where the temperature reaches over 99 % of steady state!
- **Anisotropic materials & temperature coefficients** — **Thermal Materials** manages anisotropic thermal conductivity (k_{xy}, k_z) for multilayer substrates and temperature coefficients for back-coupling ($\mathrm{TC}_{\varepsilon_r}$, copper $\mathrm{TC}_\sigma \approx -0.39\%/K$).

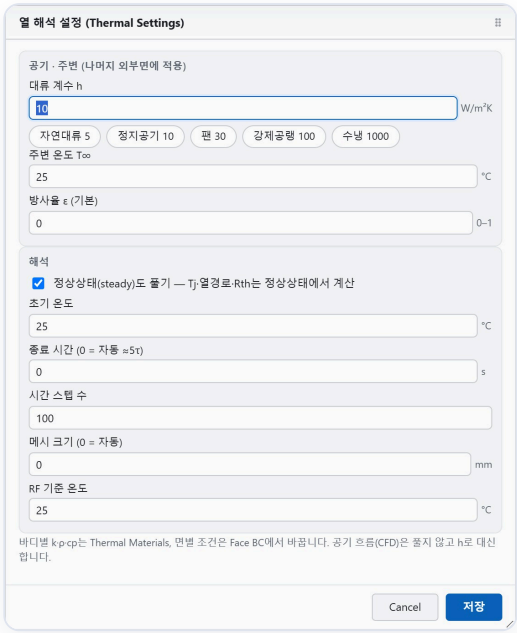


Figure 27-6 The Thermal Settings dialog. It supports one-click convection-coefficient h buttons per environment and transient analysis with an automatic time constant.

FIRST 3 MINUTES **Complete in 3 minutes as a total beginner! Follow 5 steps to your first 3D thermal analysis (thermal_chip_on_board.warp)**

1. **Open the thermal-analysis starter sample**
   In **File ▸ Open Examples...**, double-click `thermal_chip_on_board.warp` to open it.

2. **Enter the Thermal ribbon**
   Click **Thermal** in the top ribbon tabs, and the left tree changes to the dedicated thermal-workbench tree, showing the heat-generating chip · substrate · cooling boundaries.

3. **Run the one-click thermal analysis**
   Press ribbon **Thermal ▸ Run**, and within seconds the steady-state and transient temperature fields are calculated and a rainbow temperature distribution spreads across the 3D viewport.

4. **Time playback & cut-plane slice**
   In the thermal results panel on the right, press **Time ▶ Play** to watch the heat spread from the chip into the board, and turn on **Cut plane** to check the temperature gradient through the board thickness.

5. **Mouse-click temperature probe**
   Press **Pick probe point**, click the chip's top face and then the board's corner in turn, and compare the heating curves over time ($T(t)$)!

28 CHAPTER

The Three Heat Sources, Node-Split TIM and the Magic of Thin Copper



We cover the key techniques that automatically calculate heat dissipation from a transistor's datasheet operating point, connect the dielectric · skin losses of 3D EM directly as heat sources, and solve 50 μm solder and 35 μm copper foil accurately without a mesh explosion.

You will learn

Automatic Transistor heat · junction temperature Tj calculation

Try it

RF Loss → Heat, which maps pure heat only, excluding reflection · radiation

Key concepts

Zero-mesh node-split Contact/TIM and Thin Copper, which makes a 470 °C difference

28.1 Where does it get hot, and by how much? — the three heat sources (`Sources`)

① `Transistor` : P_{diss} and T_j straight from the RF operating point!

Pick the power-amplifier device body and enter the output P_{out} [W], drain efficiency η [%] and gain G [dB], and it calculates the heat loss $P_{\text{diss}} = P_{\text{out}}/\eta + P_{\text{in}} - P_{\text{out}}$ and the junction temperature $T_j = T_{\text{case,max}} + R_{\text{th,jc}} \cdot P_{\text{diss}}$ in real time.

For example, enter $P_{\text{out}} = 10\ \text{W}$, $\eta = 60\%$, $G = 15\ \text{dB}$, $R_{\text{th,jc}} = 1\ \text{K/W}$, and $P_{\text{diss}} = 6.983\ \text{W}\ (+6.983\ \text{K})$ is calculated; it sounds an alarm if the limit $T_{\text{j,max}}$ is exceeded. Ordinary resistors · heaters get volume heat (W) or surface heat flux (W/m^2) with ② `Heat Source` .



Figure 28-1 The Transistor heat source (Tj) dialog. It has 4 representative GaN/LDMOS presets and a real-time Pdiss · temperature-margin calculator built in.

② `RF Loss → Heat` : the 3D electromagnetic loss distribution, as a heat source as-is! ONLY IN AETHER

When you need to know **"which stub corner gets hottest"**, as in high-power filters, waveguide irises or dielectric-heating chambers, turn on `Save fields` in the EM Setup, run the analysis, then press ribbon **RF Loss → Heat**!

- **Automatic integration of dielectric volume loss + conductor skin loss** — it precisely maps the dielectric loss density $\frac{1}{2}\omega\varepsilon_0\varepsilon''|\mathbf{E}|^2$ inside tetrahedra and the skin-resistance loss density $\frac{1}{2}R_s|\mathbf{H}_t|^2$ on both sides of conductor sheets / walls onto each thermal body.
- **Reflected power & antenna radiated power excluded automatically!** — of the incident power P_{in}, the reflected power returned to the port ($|S_{11}|^2$) and the antenna radiated power flown off into the air (P_{rad}) don't heat the board, so they are subtracted automatically and only the pure dissipated heat is scaled exactly

(Th1 2.45 GHz 10 W dielectric-heating example: absorption 60.7 % = 6.07 W heat source → peak liquid temperature of 42.2 °C after 3 seconds, precisely reproduced).

28.2 Per-face convection · nonlinear radiation (`Face BC`) and the power of emissivity ε

After selecting faces (`F`), open **Face BC** to assign individually, to specific faces only, a fixed temperature for a liquid-cooled base, an adiabatic symmetry plane, or convection + radiation (it is remembered by normal · center coordinates, so it stays even after dimension changes!).

In particular, Stefan–Boltzmann radiative heat transfer $q_{\mathrm{rad}} = \varepsilon\sigma_{\mathrm{SB}}(T^4 - T_\infty{}^4)$ is a strongly nonlinear expression proportional to the fourth power of temperature, so the steady-state solver solves it with **an exact Newton-Raphson iteration** instead of a linear approximation. Look closely at the one-click emissivity chips: shiny polished copper (`0.03`) and raw aluminum (`0.10`) can barely radiate infrared, but **black-anodized aluminum (`0.85`)** and **solder mask (`0.90`)** become powerful radiative coolers (Chapter 31 shows the miracle!).



Figure 28-2 The face boundary condition (Face BC). It provides one-click emissivity ε chips per surface finish.

28.3 Two secret techniques that end thin-film mesh hell: `Contact / TIM` & `Thin Copper` ONLY IN AETHER

Technique ① — Node-Splitting `Contact / TIM`

Draw a 50 µm thermal-grease or SAC305 solder layer as a real thin 3D box, and millions of tetrahedra shatter and the mesh grinds to a halt. **Contact / TIM mathematically splits the FEM nodes on the interface between two touching bodies in two (node splitting) and connects them directly with the per-area thermal conductance A/R'' ($R'' = t/k$)!** With **zero** extra volume mesh, it calculates the temperature step of sintered silver (30 µm), solder, thermal grease and gap pads 100 % accurately.

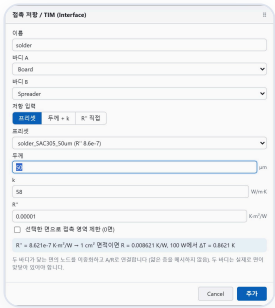


Figure 28-3 The contact thermal resistance / TIM settings window. It instantly converts and shows the temperature step ΔT produced when 100 W passes per 1 cm².

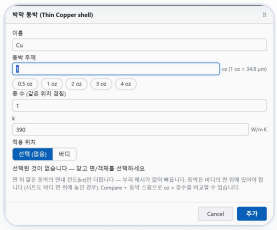


Figure 28-4 The Thin Copper settings window. It reflects the 0.5–4 oz copper thickness and the number of inner layers without a volume mesh.

Technique ② — `Thin Copper`, which lowers 595 °C to 123.5 °C!

The FR-4 dielectric itself, with a thermal conductivity of $0.3\ \mathrm{W/(m{\cdot}K)}$, is close to an insulator; the champion that actually spreads heat sideways across a real PCB is the **35 µm (1 oz) copper foil layer**, with $k = 401\ \mathrm{W/(m{\cdot}K)}$!

Give patches · ground planes drawn as zero-thickness sheets in EM a **Thin Copper** of `1 oz × number of layers`, and the tangential thermal-conduction stiffness ($k_{\mathrm{Cu}}tN$) comes alive instantly. In verification example **Th3**, leaving out the 1 oz thin copper sends the peak temperature soaring to 595 °C, but the moment you turn it on it converges exactly to the real board temperature of 123.5 °C!

HOW TO **Connect EM losses directly as heat sources! 4 essential setup steps for RF Loss → Heat & thin copper**

1. **Finish the EM analysis with Save fields**
   In the EM `Frequency Sweep`, finish the `F9` analysis with `Save fields` checked at the operating frequency where you want to see the heating.

2. **Assign Thin Copper first!**
   Move to the **Thermal** ribbon, open **Thin Copper** and give the sheet conductors (signal lines · ground planes) their real copper thickness (e.g. `1 oz = 35 µm`) (leave it out and the lateral heat spreading goes missing, so the temperature spikes abnormally!).

3. **Connect the TIM contact resistance**
   Between a touching chip and pad, or board and heatsink, assign solder (`SAC305`) or thermal grease with **Contact / TIM**.

4. **RF Loss → Heat mapping & Run**
   Open ribbon **RF Loss → Heat**, enter the real applied RF power (e.g. `Pin = 10 W`) to register it as a heat source, then press **Run**!

29 CHAPTER

Practical Guide to the Five Cooling Helpers: Thermal Via · Copper Coin · Spreader · PCM · Pulse



When a device runs hot, don't reach for a fan first! From anisotropic thermal vias that suit a 4 W-class QFN perfectly, to the copper coin that saves a 220 W-class LDMOS, to the phase-change material (PCM) that shaves radar burst peaks, we compare the best prescription for each situation.

You will learn
The cooling-helper selection matrix by heat scale

Try it
The anisotropic-homogenizing Via Wizard (Th4: 272.7 → 75.9 °C)

Key concepts
Copper coin (Th2) · spreader (Th5) · PCM latent heat & pulse integration (Th6)

29.1 Which cooling helper is the right answer for my circuit?

Cooling helper	Recommended heat scale	Key working principle · practical applications
Thermal Via Wizard	Low to medium power ($1 \sim 15$ W)	Drives a grid of plated · copper-filled vias into QFN/SOIC pads on FR-4/RO4350B boards to pull heat down to the bottom heatsink.
Copper Coin / cutout	High power ($15 \sim 300$ W+)	Under high-power GaN/LDMOS that even vias can't handle, it pierces the board and connects a solid copper block (coin) or pedestal directly.
Heat Spreader	Sealed modules · shield cans	Connects an idle metal shield can or the ceiling of an aluminum enclosure with thermal pads (TIM), widening the cooling area several times over.
PCM + Pulse / Duty	Intermittent bursts · radar	When the average power is low but high power bursts for a few seconds, it pins down the peak temperature with the **latent heat of fusion (Latent Heat)** of paraffin · gallium!

29.2 Compare and homogenize hundreds of vias in 1 second: `Thermal Via Wizard` (Th4 verified)

Drill 100 vias one by one as cylinder solids, and the mesh alone grows by hundreds of thousands. **Via Wizard** lines up as many as 4 via processes (drill diameter d, pitch p, plating thickness, resin vs copper fill) side by side, calculates **the through-thickness k_z with the exact area-parallel law** and **the lateral k_{xy} with the Maxwell–Rayleigh effective-medium formula**, and swaps them at top speed for a single anisotropic block!

Th4 verification (4 W QFN on FR-4)	Junction temp. T_j	Improvement
No thermal vias (bare FR-4)	**272.7 °C**	Device burns out instantly
$d = 0.3$ mm, $p = 1.0$ mm **resin fill**	100.7 °C	−172.0 K plunge!
$d = 0.3$ mm, $p = 0.6$ mm **copper fill**	77.4 °C	Tight pitch + Cu fill
$d = 0.5$ mm, $p = 0.8$ mm **copper fill**	**75.9 °C**	Comfortable mass-production margin

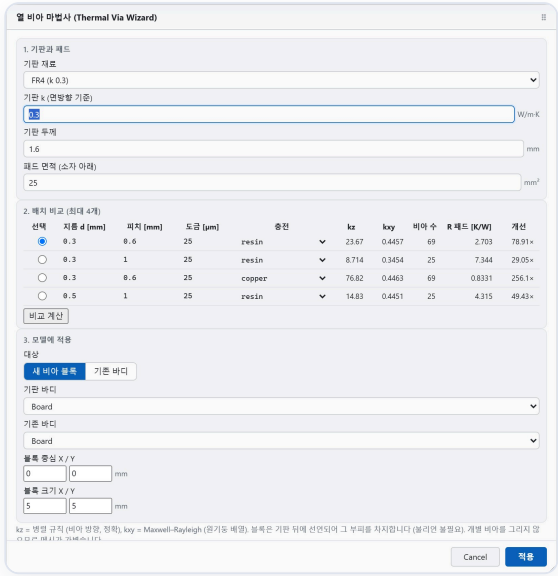


Figure 29-1 The Thermal Via Wizard. It compares the equivalent kz · kxy per process and the pad thermal-resistance improvement factor at a glance in a table.

29.3 The direct high-power highway: `Copper Coin` (Th2) & `Heat Spreader` (Th5)

`Copper Coin` creates, in one click, a copper block through the board, its design variables (`Coin_w`, `Coin_l`), and even the `SAC305 50 µm` solder TIM under the device. In the Th2 example, where a 500 W-class LDMOS pours out **220.6 W** of heat loss, the board alone would theoretically burn at 2404 °C, but once the copper coin is driven in and connected directly to the cold plate it is perfectly controlled at $T_j = 104.5\ ^\circ C$!

`Heat Spreader`: pick a shield-can or metal-enclosure body, and it fastens a wildcard TIM (`a = *`) to every touching internal part in one go. In the **Th5** example, connecting the shield can **halved it from 315.5 °C → 150.6 °C**, and switching the board to aluminum nitride (AlN) brought it down to 63.6 °C.



Figure 29-2 The Copper Coin creation window. It links directly to automatic dimension optimization with Optimize Tj later on.

29.4 Swallowing burst peaks with latent heat: `PCM` & `Pulse / Duty` (Th6 verified)

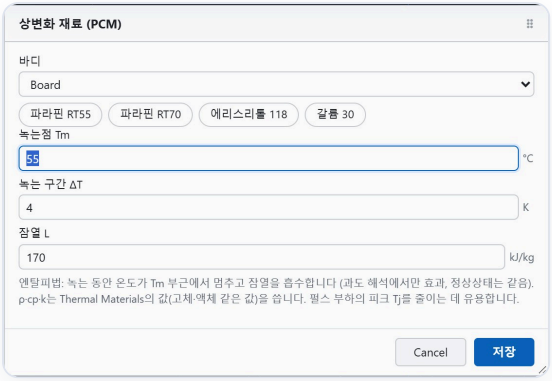


Figure 29-3 Phase-change latent-heat material (PCM) settings. It has built-in presets for paraffin RT55/RT70, erythritol (118 °C) and gallium (29.8 °C).

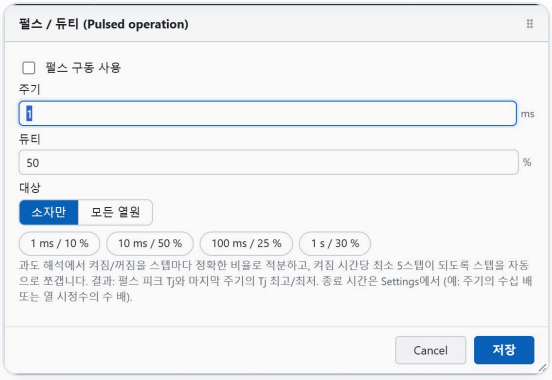


Figure 29-4 Pulse / Duty settings. It automatically places at least 5 time steps in every ON interval, preventing missed pulse peaks at the source.



Thermy's cooling · thermal-analysis coaching

Just as ice stays at 0 °C until it has all melted, **a phase-change material (PCM)** absorbs heat near its melting point T_m with a huge latent heat of fusion L (enthalpy method)! In the 6-second-period, 50 % duty burst example (**Th6**), a single paraffin block pushes the peak T_j down from **114.9 °C → 103.3 °C (−11.6 K peak cut!)**. However, in continuous steady-state operation the latent heat is used up, so use it for intermittent burst systems!

30 CHAPTER

Thermal-Bottleneck Tracing (Heat Path) · Auto-Optimization · Temperature → RF Two-Way Coupling



Master Heat Path, which points out with a single bar where a fix will drop the temperature the most; Optimize Tj, which finds by bisection the smallest copper-coin width that keeps Tj under target; and Temp → RF, which feeds back how far a heated dielectric pushes the resonant frequency.

You will learn

3D temperature cut planes · probes · energy-conservation (<10^{-12} W) verification

Try it

Per-segment Heat Path bottleneck diagnosis and Compare sweeps

Key concepts

Bisection Optimize Tj (Th8) and Temperature → RF convergence (Th7)

30.1 3D temperature field · time slider · pinpoint `Heat Path` bottleneck diagnosis

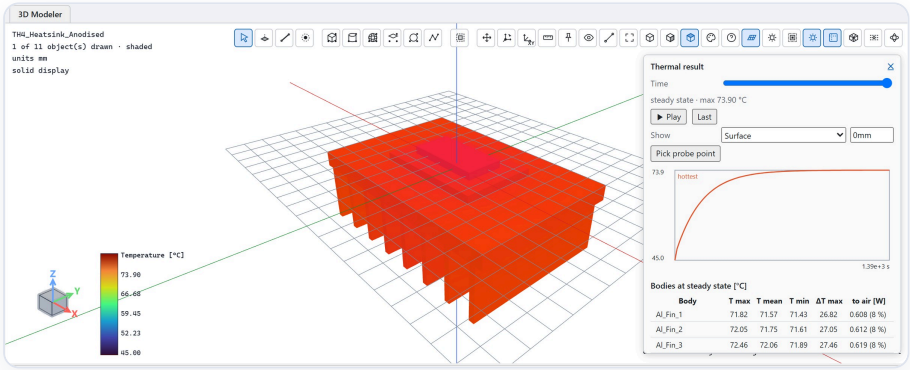


Figure 30-1 The finished thermal-analysis screen for Th2 (220.6 W LDMOS + copper coin). In the right panel, check transient time playback, cut-plane slices, click-probe temperature curves and each body's share of heat released to the air.

Right after the analysis, the Message Manager records **the energy-conservation balance error** ($|\text{input W} - (\text{convection} + \text{radiation} + \text{heat storage} + \text{fixed-face outflow})| < 10^{-12}$ W) and the thermal time constants τ_{63}, t_{90}. The window you must open next is ribbon **Heat Path**!

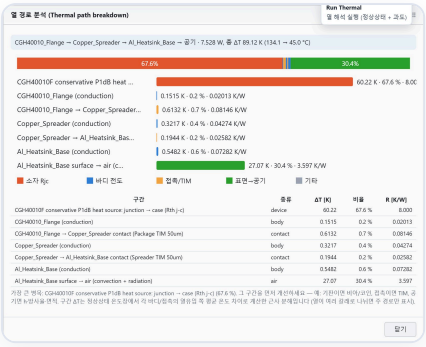


Figure 30-2 The Heat Path thermal-path bottleneck breakdown chart. It intuitively breaks down the ΔT (K) and share (%) each segment eats up, from the device's internal Rjc to the solder, coin and chassis.

Heat Path, which saves you from fixing the wrong place

Look at the Th2 thermal-path bars on the left! Of the total temperature rise $\Delta T = 64.23\ \mathrm{K}$, a whopping **61.8 % occurs in the transistor package's internal thermal resistance** $R_{\mathrm{th,jc}}$, and the steps across the copper coin and chassis segments are very small.

In other words, in this state doubling the board's copper coin or increasing the coolant flow won't lower T_j by more than a few degrees! In 3 seconds you reach the conclusion that if you need a lower T_j, you must pick a higher-grade device with a smaller package R_{jc} or split the power in parallel across 2 devices.

30.2 Reading thermal results the easy way: safe temperature criteria & a 1-second prescription table by bottleneck

Once the thermal analysis is done, decide instantly with the single practical judgment table below whether the numbers are safe or dangerous, and which part to fix.

Check item · bottleneck segment	Practical safety criterion · signal	Cause diagnosis & the most effective immediate prescription
GaN / Si device junction T_j	GaN $\leq 150 \sim 175\ ^\circ\mathrm{C}$ Si / LDMOS $\leq 125 \sim 150\ ^\circ\mathrm{C}$	A margin of at least $25 \sim 50\ \mathrm{K}$ below the absolute rating (200–225 °C) is mandatory (MTTF lifetime scales exponentially!).
PCB substrate peak temperature	Standard FR-4 $\leq 105 \sim 115\ ^\circ\mathrm{C}$ (glass transition $T_g \approx 135\ ^\circ\mathrm{C}$)	Near T_g, substrate delamination · $tan\ \delta$ blows up! Switch hot spots to RO4350B / ceramic (AlN) or add `Thin Copper` 2 oz.
`Heat Path` **#1: substrate (PCB)**	Substrate-segment ΔT share is largest	No vertical heat path → **copper-filled thermal vias** below 15 W, and **a copper coin / cutout jig connected directly** above 15 W!
`Heat Path` **#1: air (Air)**	Heatsink surface → T_∞ step is largest	Poor radiation from bare silver metal in still air → **black anodizing ($\varepsilon = 0.85$)** + more fin area, or a small fan ($h \uparrow$).
`Heat Path` **#1: device R_{jc}**	Package-internal $\Delta T > 50\%$	External cooling has already hit its limit! Switch to a higher-grade package with a lower R_{jc}, or split across 2 devices balanced / Doherty.
Transient τ_{63} & energy error	Balance error $< 10^{-12}\ \mathrm{W}$	If the burst width $< \tau_{63}$, a **PCM latent-heat material** effectively suppresses peaks; for continuous operation, cutting the steady-state thermal resistance (R_{th}) is a must.

30.3 What-If batch comparison (`Compare / Sweep`) and target `Optimize Tj` (Th8 verified)

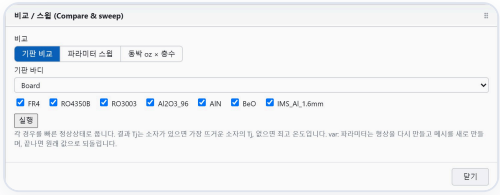


Figure 30-3 Compare / Sweep. It compares FR-4 · RO4350B · Al_2O_3 · AlN · IMS substrate swaps or a copper oz × layer-count matrix in seconds.



Figure 30-4 Automatic target-Tj optimization (Optimize Tj). With monotonic bisection, it finds the optimal design variable exactly within at most 14 thermal analyses.

Optimize Tj automatically searches by monotonic bisection for **"what is the smallest copper-coin width (`Coin_w`), or the widest allowable via pitch, that satisfies a junction temperature $T_j \le 130$ $^\circ$C?"**. In verification example **Th8** (a 300 W-class device), after just 10 thermal analyses it automatically found the minimum coin width `Coin_w = 5.83 mm` ($T_j = 129.6$ $^\circ$C) that just barely holds the 130 °C target!

30.4 A heated resonator pushes its frequency away: `Temp → RF` two-way coupling (Th7) ONLY IN AETHER

When a high-power filter or ceramic resonator heats up, the substrate permittivity $\varepsilon_r(T)$ changes so that the resonant frequency itself drifts sideways ($\Delta f/f \approx -\frac{1}{2}\Delta\varepsilon_r/\varepsilon_r$), and the copper conductivity $\sigma(T)$ drops so that insertion loss grows.

CLOSED LOOP **3 steps of Temperature → RF two-way convergence**

1. **EM (Save fields) → RF Loss → Heat → Run Thermal**
   Obtain the first EM losses and 3D temperature field with room-temperature (25 $^\circ$C) properties.

2. **Thermal ▶ Temp → RF ▶ Apply to materials**
   Check the derived materials corrected to each body's average temperature (`<name>_T31C` etc., with built-in protection against duplicate stacking!) and the predicted frequency shift (ppm), then apply.

3. **Check re-analysis convergence**
   Run `F9` EM re-analysis → `RF Loss → Heat` update → `Run Thermal` . The high-power dielectric-heating resonator example (**Th7**, ε_r: $24.0 \to 23.43$ thermal drift) **converges completely in just 2 iterations, with a temperature change** < 0.5 K!

The thermal workbench's physical limits, stated honestly (Solid FEM vs CFD)

Aether's thermal solver is **a solid-conduction FEM + surface convection coefficient h + Newton nonlinear radiation** solver; it is not CFD (computational fluid dynamics) that solves the Navier–Stokes flow field of the air itself. For example, if you pack natural-convection heatsink fins tightly at 1 mm spacing, the air actually chokes (boundary-layer choking) and cooling gets worse, but with a fixed h the temperature may be calculated as lower because the area grew. Keep natural-convection fin spacing at least 5–6 mm, and enter a realistic h that matches the correlations.

31 CHAPTER

[Special Feature] Integrated Electro-Thermal Cooling Design of a GaN PA and the Metal Jig



We reveal the practical secret that lowered a GaN PA's temperature by 26.1 K and passed the production spec with nothing but a black-anodized surface finish (ε = 0.85) — no noisy, failure-prone cooling fan — along with how to diagnose thermal runaway (DE tempco) and how to design a board-cutout aluminum jig!

You will learn

3-point nonlinear thermal-FEM Rca(P) characterization

Try it

DE tempco, which catches real thermal runaway behind the gain-tempco illusion

Key concepts

The black-anodizing −26.1 K miracle (TH1–TH4), the cutout cooling jig + avoiding cavity resonance

31.1 Why did the same aluminum heatsink drop 26.1 °C just by turning it black?

The shipped example `pa_v2/CGH40010_5g8_PA_Results_Thermal_v2.warp` holds, in a single project, **4 cooling designs (`TH1` – `TH4`)** for a 5.8 GHz 10 W-class GaN HEMT (`CGH40010`, operating-point heat $P_{\mathrm{diss}} = 7.53\ \mathrm{W}$, midsummer ambient $T_{\infty} = 45\ ^{\circ}\mathrm{C}$, safety limit $T_{\mathrm{j,max}} = 150\ ^{\circ}\mathrm{C}$).

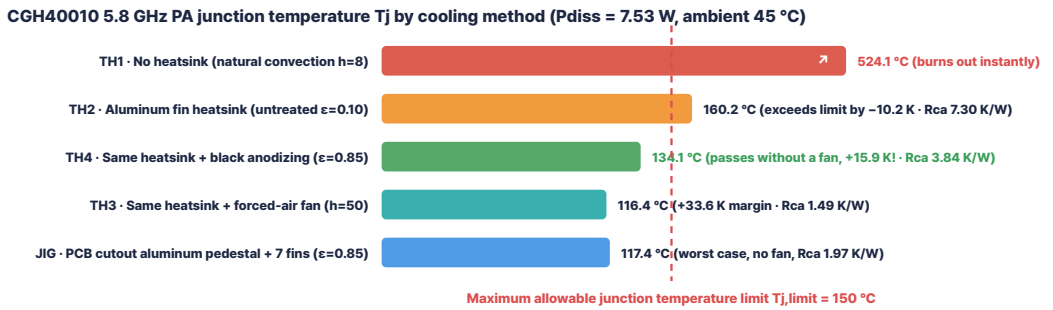


Figure 31-1 FEM comparison of the case-to-air thermal resistance Rca and final junction temperature Tj for the TH1–TH4 cooling methods on the CGH40010 GaN PA (7.53 W heat, 45 °C ambient).

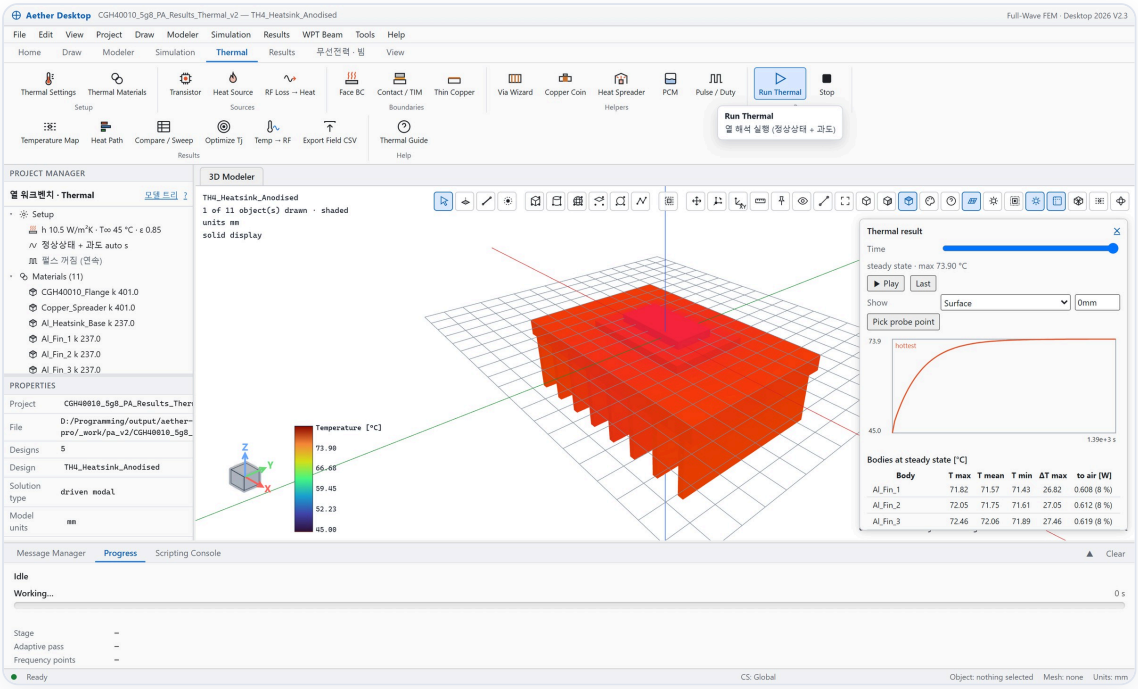


Figure 31-2 The 3D thermal-analysis result of the TH4_Heatsink_Anodised design. Even in fanless natural convection (h = 10.5 W/m²K), thanks to black-anodized radiation (ε = 0.85), the heatsink peak temperature settles at 73.9 °C and the chip's internal junction temperature Tj at 134.1 °C (a +15.9 K margin against the limit!).

Cooling design	Condition summary	R_{ca} (K/W)	Final T_j ($T_{amb} = 45\ ^\circ C$)	Verdict (150 °C limit)
TH1 No Heatsink	Bare board exposed, no heatsink	55.65	**524.1 °C**	Burns out instantly (−374 K)
TH2 Heatsink Natural	Untreated silver machined aluminum fins ($\varepsilon = 0.10$, still air)	7.30	**160.2 °C**	**Fails spec (exceeds by −10.2 K!)**
TH4 Heatsink Anodised	**100 % identical shape to TH2 + black anodizing ($\varepsilon = 0.85$)**	**3.84**	**134.1 °C**	**Passes without a fan! (+15.9 K margin, −26.1 K saved!)**
TH3 Heatsink Forced	Forced-air fan attached (h raised)	1.49	**116.4 °C**	Passes (+33.6 K margin; beyond this, $R_{jc} = 8$ is the bottleneck)



Thermy's cooling · thermal-analysis coaching

In outdoor base stations or silent equipment without a forced-air fan, natural convection alone removes only half the heat! Silver machined aluminum ($\varepsilon = 0.10$) traps infrared like a mirror, but just apply an inexpensive **black-anodized surface finish ($\varepsilon = 0.85$)** and the infrared radiative cooling explodes from $0.56\ \mathrm{W} \rightarrow 2.77\ \mathrm{W}$ **(about 5×!)**, halving the thermal resistance R_{ca} from $7.30 \rightarrow 3.84\ \mathrm{K/W}$ and shaving off 26.1 K without a single fan!

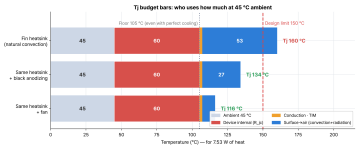


Figure 31-3 ① The floor of the thermal budget (105 °C): adding just the package Rjc (8 K/W × 7.53 W = 60.2 K) to 45 °C air already gives 105.2 °C! The heatsink Rca must be 5.95 K/W or less to survive.

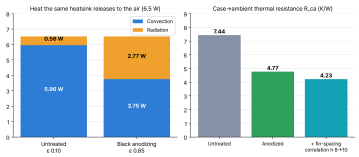


Figure 31-4 ② The physics of black anodizing: the shape stays the same, yet the infrared radiation output jumps 5× from 0.56 W → 2.77 W, shaving off 26.1 K!

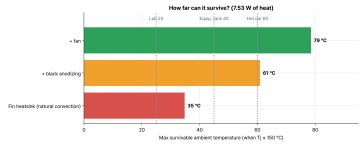


Figure 31-5 ③ The highest survivable ambient temperature per cooling option: TH2 (untreated) fails at 34.8 °C, but TH4 (anodized) holds out up to 60.9 °C — even through a heat wave!

31.2 The secrets of `Heat and cooling` and `DE tempco` thermal runaway in the PA Tuner! NEW V2.3 ONLY IN AETHER

In the `PA Results` window, expand section `4 · Heat and cooling` and press the **Characterise cooling designs** button, and it solves each of the project's `TH1` – `TH4` designs with a 3-point thermal FEM at $0.5\times$, $1\times$, $1.5\times$ heat and registers **an $R_{ca}(P)$ interpolation curve** that keeps the radiation · natural-convection nonlinearity alive (every time you change the input power, the T_j curves of all heatsinks are drawn at once in 0.1 seconds!).

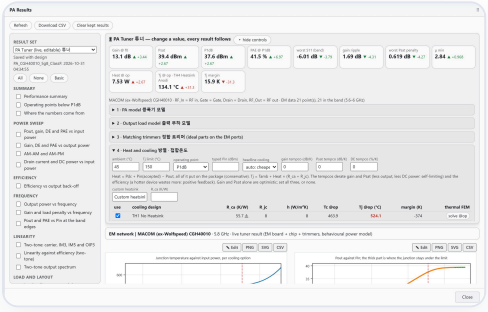


Figure 31-6 The Heat and cooling section of PA Results. It diagnoses the junction-temperature curve versus input power and the safe output range in real time.

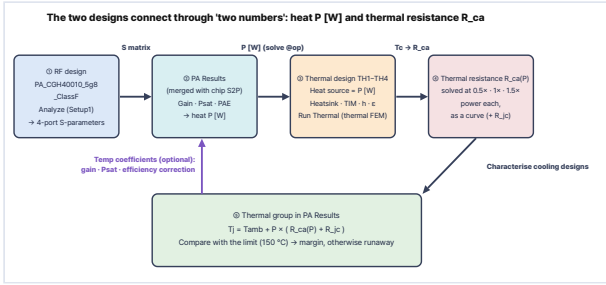


Figure 31-7 The nonlinear Rca(P) interpolation curve extracted by a 3-point (0.5×, 1×, 1.5× heat) thermal FEM. It even captures how the thermal resistance gently falls as temperature rises and the radiation (T^4) share grows.

CREW COMIC **A must-read for experts — why can't gain temperature coefficients alone ever catch thermal runaway?**



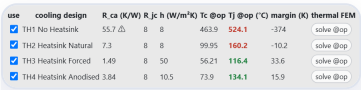
Porty Thermy! When the temperature rises, GaN gain and saturated power drop, so I entered only `gain tempco = -0.015 dB/K` and `Psat tempco = -0.01 dB/K`, and the temperature rose a bit and then stopped on its on. Safe, right?

Thermy That's dangerous talk!! If you turn on only the negative gain and P_{sat} coefficients, output and DC current drop together as temperature rises, so the heat drops too — **a fake self-limiting (an optimistic illusion)**!



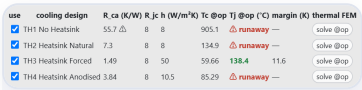


Wiz Exactly! In reality, the hotter the device gets, **the more the drain efficiency (DE) itself erodes**, so it pours out more heat to deliver the same output — **a positive feedback (Positive feedback = thermal runaway!)**. As in the 3-step measured comparison below, you must enter all three together, **including** `DE tempco` **(e.g.** `-0.15 %/K` **)**, to catch the real `⚠ thermal runaway` threshold!



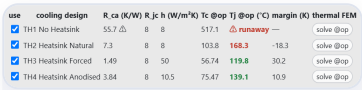
use	cooling design	R_ca (K/W)	R_jc	h (W/m²K)	Tc @op	Tj @op (°C)	margin (K)	thermal FEM
☑	TH1 No Heatsink	55.7 ⚠	8	8	463.9	524.1	-374	solve @op
☑	TH2 Heatsink Natural	7.3	8	8	99.95	160.2	-10.2	solve @op
☑	TH3 Heatsink Forced	1.49	8	50	56.21	116.4	33.6	solve @op
☑	TH4 Heatsink Anodised	3.84	8	10.5	73.9	134.1	15.9	solve @op

Figure 31-8 ① Temperature coefficients OFF (Cold): calculated with a fixed heat only, so no sign of thermal runaway shows at all.



use	cooling design	R_ca (K/W)	R_jc	h (W/m²K)	Tc @op	Tj @op (°C)	margin (K)	thermal FEM
☑	TH1 No Heatsink	55.7 ⚠	8	8	905.1	⚠ runaway	—	solve @op
☑	TH2 Heatsink Natural	7.3	8	8	134.9	⚠ runaway	—	solve @op
☑	TH3 Heatsink Forced	1.49	8	50	59.66	138.4	11.6	solve @op
☑	TH4 Heatsink Anodised	3.84	8	10.5	85.29	⚠ runaway	—	solve @op

Figure 31-9 ② DE tempco (−0.15 %/K) alone ON: through the efficiency-drop → heat-rise loop, TH1 · TH2 · TH4 run away in a chain!



use	cooling design	R_ca (K/W)	R_jc	h (W/m²K)	Tc @op	Tj @op (°C)	margin (K)	thermal FEM
☑	TH1 No Heatsink	55.7 ⚠	8	8	517.1	⚠ runaway	—	solve @op
☑	TH2 Heatsink Natural	7.3	8	8	103.8	168.3	-18.3	solve @op
☑	TH3 Heatsink Forced	1.49	8	50	56.74	119.8	30.2	solve @op
☑	TH4 Heatsink Anodised	3.84	8	10.5	75.47	139.1	10.9	solve @op

Figure 31-10 ③ All 3 tempcos (Gain · Psat · DE) ON: real physics converges! Only TH1 runs away, and TH4 survives at 139.1 °C!

31.3 The practical hardware standard: board-cutout (Cut-out) aluminum metal-jig design

When testing or mass-producing a 25 W-class packaged transistor (`pa_cg2h40010_5g8_jig.warp`), the surest cooling structure is one that **doesn't pass through the poorly conducting PCB substrate at all!**

- **PCB center cutout + direct pedestal connection** — cut a rectangle out of the board center, and bolt the transistor's copper flange directly, with thermal grease ($50\ \mu\mathrm{m}$), onto the top of a pedestal rising from the aluminum jig base. Only the input · output leads are soldered to the microstrips on the RO4350B boards on either side.
- **Performance of the 7-fin black-anodized natural-convection jig** — with 6 mm fin spacing ($h \approx 10.1\ \mathrm{W/m^2K}$ correlation) and $\varepsilon = 0.85$ applied, it achieves a whopping $R_{\mathrm{ca}} = 1.97\ \mathrm{K/W}$ with no fan! At a standard 4.71 W of heat $T_j = 92.0\ ^\circ\mathrm{C}$, and even in the worst case of 7.26 W · 45 °C ambient it holds out easily at $T_j = 117.4\ ^\circ\mathrm{C}$.
- **Electromagnetic trap warning — metal-lid cavity resonance!** — cover this $28 \times 35\ \mathrm{mm}$ metal jig with a metal shielding lid, and the air space inside becomes **a 6.0–6.9 GHz TE_{101} cavity resonator**, disturbing the 5.8 GHz PA gain and inviting oscillation! Leave the jig open on top, or if shielding is a must, attach an EM absorber sheet (Chapter 13 Impedance boundary) inside the lid and always verify it together in 3D FEM.

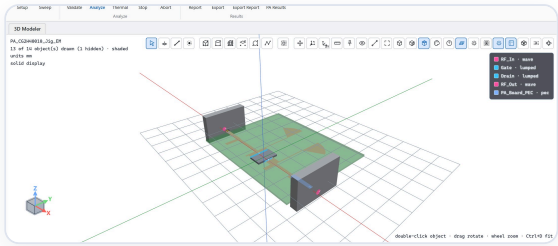


Figure 31-11 The 3D model of a 5.8 GHz CG2H40010 Class-F PA mounted on a board-cutout aluminum cooling jig (pa_cg2h40010_5g8_jig.warp).

PART

07

Practical Design Tutorial Masterclass From a Blank Ctrl+N Coordinate Sheet to the 8 GaN PA Missions

A manual you only read with your eyes is forgotten the moment you close it, but the experience of typing dimensions with your own fingertips and pushing the sliders yourself becomes an engineer's weapon for life. In Part 7, following the click order exactly, you fully absorb an expert's practical sense — from a beginner lab that completes an antenna from scratch on a blank sheet (Ctrl+N) using only Tab coordinate input, to 1×4 array auto-feed and the 80 GHz radar phase-reversal incident, 1-pass space mapping (Solved at) in the shape playground, WPT rectenna schematic back-annotation, and the 8-step detective missions of the CGH40010 · CG2H40010 GaN power amplifiers, all the way to metal cooling-jig design.



32 Tutorial 1 (Beginner) · Dipole & Patch Antenna Drawn by Coordinates from a Blank Sheet (Ctrl+N)

33 Tutorial 2 (Lower-Intermediate) · 1×4 Array Auto-Feed · Real-Time Beam Steering · The 80 GHz Phase Incident

34 Tutorial 3 (Intermediate) · Shape Playground (rf_shapes_playground) & Mastering 1-Pass Space Mapping

35 Tutorial 4 (Upper-Intermediate) · 5.8 GHz WPT Rectenna + 7-Port Rectifier HB & Schematic Back-Annotation

36 Tutorial 5 (Expert Missions) · CGH40010 5.8 GHz GaN PA Tuner Adventure

37 Tutorial 6 (Flagship R&D) · CG2H40010 −33 % Miniaturization · Parasitic Audit · Metal Jig Design

32 CHAPTER

Tutorial 1 (Beginner) · Dipole & Patch Antenna Drawn by Coordinates from a Blank Sheet (Ctrl+N)



Going beyond opening shipped files, you complete two reference antennas from start to finish yourself on an empty screen, using only keyboard coordinate input: a 3 GHz half-wave dipole that verifies the solver's accuracy, and a 5.8 GHz FR-4 patch antenna that exposes the matching illusion.

You will learn
Starting from a blank Ctrl+N sheet · exact mm coordinate-input practice

Try it
One-click Port (pick) feeding vs the theoretical directivity (2.15 dBi)

Key concepts
Checking FR-4 dielectric loss (η = 46 %) and the 30-second Antenna Designer check

LAB 32-A · ZERO TO FIRST ANTENNA

Difficulty ★☆☆ · 12 min

Lab A: Complete a 3 GHz half-wave dipole antenna yourself from an empty project

Goal: build the two conductor arms and the 2 mm feed sheet to exact values, and confirm with your own hands agreement within 0.04 dB of the theoretical directivity (2.15 dBi).

32.1 Step 1 · Create a new project and enter the coordinates of 4 shapes

Press `Ctrl`+`N` (**File ▶ New Project**) to open a blank design. Check that the unit on the right of the status bar is `mm`, then open **Draw ▶ Box...** and **Draw ▶ Rectangle...** from the top menu and enter the numbers in the table below in order. The 3 GHz free-space wavelength is $\lambda_0 = 99.93\ \text{mm}$; allowing for the end fringing capacitance of the 2 mm-thick conductor arms, the total length is set to $0.417\ \lambda_0 \approx 41.66\ \text{mm}$.

Object name	Command (plane)	Start position `(X, Y, Z)` [mm]	Size `(dX, dY, dZ)` [mm]	Material / role
Arm_Top	Box	`(-1, -1, 1)`	`(2, 2, 19.83)`	`pec` (upper conductor arm)
Arm_Bottom	Box	`(-1, -1, -20.83)`	`(2, 2, 19.83)`	`pec` (lower conductor arm)
Feed	Rectangle (XZ)	`(-1, 0, -1)`	`dX = 2, dZ = 2`	Sheet (feed-gap bridge)
Air	Box	`(-50, -50, -70)`	`(100, 100, 140)`	`vacuum` ($\geq \lambda_0/2$ clearance)

The trick to drawing fast with mouse + `Tab`: press the **Box** icon on the ribbon, then press `Tab` right away, before clicking the viewport, and the cursor jumps into the numeric input box on the left. Type `-1, -1, 1` → `Enter` → size `2, 2, 19.83` → `Enter`, and it is created exactly to 0.01 mm with no mouse jitter!

Name it `Air` and its material automatically becomes `vacuum` and it is rendered semi-transparent, so you can see the dipole inside clearly.

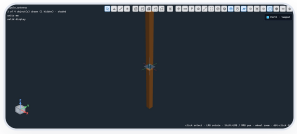


Figure 32-1 The finished 3 GHz dipole shape (identical to the shipped dipole_antenna.warp). The red sheet in the center (Feed) is the 50 Ω Lumped Port.

32.2 Step 2 · Port · absorbing boundary · local mesh · Setup (click by click!)

1. **Assign a 50 Ω Lumped Port**
   In the tree, right-click the `Feed` sheet → open **Assign Excitation ▶ Lumped Port...**. Set the resistance to `50` Ω and the integration direction (Direction) to `+Z` (lower arm $z=-1$ → upper arm $z=+1$), then press **OK**. (Or press ribbon **Port (pick)**, click the bottom face of `Arm_Top` → click the top face of `Arm_Bottom` → press **Apply**, and creating the `Feed` sheet and assigning the port finish together in 3 seconds!)

2. **Radiation open boundary**
   In the tree, right-click `Air` → choose **Assign Boundary ▶ Radiation** to wrap all 6 outer faces in a free-space absorbing boundary.

3. **Reinforce the local mesh at the feed gap**
   Right-click `Feed` → in **Assign Mesh Operation ▶ On Selection...**, set a maximum edge length of `1.0mm` (`2.5mm` recommended for the conductor arms).

4. **Add a Setup & Sweep, then run `F9`!**
   In **Simulation ▶ Add Solution Setup...**, choose frequency `3GHz`, Max passes `3`, $\Delta S = 0.02$, Basis order `Second order`, then add a `2.6GHz` – `3.4GHz` sweep (`Interpolating` or `Fast`, with `Save fields` checked!). Confirm the `F5` check passes, then press `F9`!

32.3 Step 3 · Reading the results and comparing with physical theory

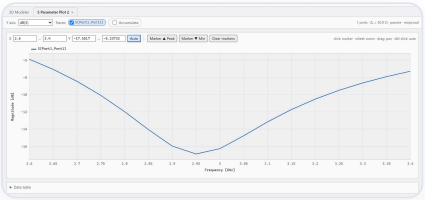


Figure 32-2 The S11 curve of your own dipole. It resonates at 2.95 GHz at −16.89 dB with a generous 16.2 % bandwidth.



Figure 32-3 The 3D radiation pattern (Results ▶ Far Field ▶ 3D pattern). The ±z-axis nulls and the 2.19 dBi peak in the equatorial plane are clear.

- **Verified within 0.04 dB of the theoretical solution** — open **Results ▶ Far Field Radiation Pattern...** and it shows **a maximum directivity of 2.19 dBi** ($\theta = 90^\circ$) and **100 % radiation efficiency**. That is a mere 0.04 dB from the exact half-wave dipole solution in electromagnetics textbooks **(2.15 dBi)**!
- **Watch a living standing-wave current** — turn on **Results ▶ Surface Current |Js|** and press **Instantaneous + ▶ Animate** in the right panel. A half-wave standing wave pulses before your eyes, with the current at its maximum at the center feed and pinned exactly to 0 at the open ends on both sides ($z = \pm 20.83$ mm).

LAB 32-B · PATCH FROM SCRATCH & WIZARD RACE

Difficulty ★☆☆ · 15 min

Lab B: 5.8 GHz FR-4 patch antenna by hand vs a 30-second Antenna Designer showdown!

Goal: draw a patch on a low-cost FR-4 board by coordinates, confirm the 'matching illusion' where S11 = −20 dB yet half disappears as heat, and compare with the wizard's auto-tuning.

32.4 Step 1 · Coordinate table for a 5.8 GHz probe-fed patch (same specs as `patch_antenna.warp`)

Open a new design and enter the 4 objects below (substrate: `FR4_epoxy`, $\varepsilon_r = 4.4$, $tan\ \delta = 0.02$, $h = 1.6$ mm). Stand a vertical feed-ribbon sheet at $x = 2.77$ mm, inset 2.7 mm inward from the radiating edge ($x = +5.47$ mm).

Object name	Command (plane)	Start position `(X, Y, Z)` [mm]	Size [mm]	Boundary / port assignment
Substrate	Box	`(-16, -16, 0)`	`(32, 32, 1.6)`	Material `FR4_epoxy` · **Perfect E (Ground)** on the bottom face ($z = 0$)
Patch	Rectangle (XY)	`(-5.47, -7.85, 1.6)`	`10.94 × 15.7`	Right-click the sheet → **Perfect E** ($L_p = 10.94$, $W = 15.7$ mm)
Feed	Rectangle (YZ)	`(2.77, -0.5, 0)`	`dY=1.0, dZ=1.6`	**Lumped Port** (50 Ω, `+Z` direction)
Air	Box	`(-29, -29, 0)`	`(58, 58, 17.1)`	Assign `Radiation` to only the 5 outer walls, excluding the bottom ($z = 0$)!

Run `Setup1` (`5.8GHz`, 5 passes, second order) and a `5.3~6.3GHz` sweep, and S_{11} matches perfectly at -20.3 dB **@ 5.75 GHz** (-19.9 dB at 5.8 GHz; -28.5 dB for the 2.45 GHz version). But the moment you open the far-field table, you're in for a shock!

Because of FR-4's large dielectric loss ($tan\ \delta = 0.02$), more than half of the electric-field energy trapped under the resonant patch is consumed as heat, and **the radiation efficiency only reaches $\eta_{\text{rad}} \approx 46\%$ (3.38 dB of gain evaporates relative to directivity!)**.

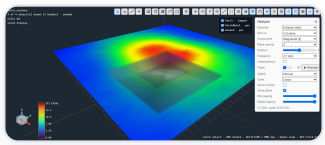


Figure 32-4 The |E| distribution in the patch cross-section. A strong electric field is trapped inside the FR-4 under both radiating slots, causing dielectric heat loss.

A beginner's lifelong rule: even a 50 Ω dummy resistor gives $S_{11} = -\infty$ dB on a VNA! An antenna only truly passes once you've checked its **Realized Gain** and **radiation efficiency (η_{rad})**. Now open **Draw ▸ Antenna Designer...** ONLY IN AETHER, change only the substrate to `RO4003C` and press `Auto-tune (FEM)` — the patch I spent 15 minutes fitting is finished after a single automatic correction, at **5.804 GHz**, $S_{11} = -23.8$ dB**, efficiency 80 %+**!

33 CHAPTER

Tutorial 2 (Lower-Intermediate) · 1×4 Array Auto-Feed · Real-Time Beam Steering · The 80 GHz Phase Incident



Bundle 4 single patches to raise the gain to 12.2 dBi, and finish distribution-network wiring that used to take two days in 1 minute with Auto Feed + Feed Tune. Then steer the beam without re-analysis using Edit Sources, and solve the hair-raising phase-reversal incident of an 80 GHz automotive radar array!

You will learn

RO4003C 1×4 corporate feed and Feed Tune (11.7° → 1.45°)

Try it

Real-time beam steering with Edit Sources, no re-analysis, and finite-ground side lobes

Key concepts

The cause of the 80 GHz 2×2 array's broadside beam split (−4.8 dBi) and the U-shaped delay-line fix

LAB 33-A · CORPORATE FEED & FEED TUNE

Difficulty ★★☆ · 15 min

Lab A: Analyzing a 5.8 GHz 1×4 array and one-click Auto Feed Network synthesis

Target sample: `examples/patch_array_1x4_5g8.warp` + `Auto Feed Network` ONLY IN AETHER

First open the shipped example `patch_array_1x4_5g8.warp` and run `F9`. On low-loss `RO4003C` ($h = 0.813$ mm, $tan\ \delta = 0.0027$), 100 Ω inset feed lines gather at the center port through T-junctions (50 Ω) and $\lambda_g/4$ transformers (70.7 Ω).

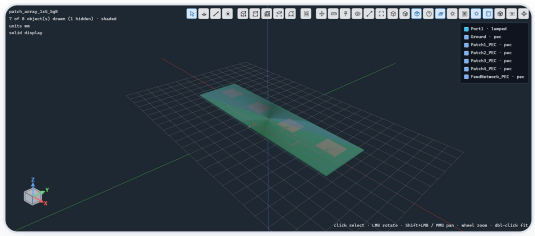


Figure 33-1 The 5.8 GHz 1×4 corporate-fed patch array on an RO4003C board (patch_array_1×4_5g8.warp).

- **See the power of the fast ROM sweep** — the log at the bottom shows that of the 41 frequency points, the solver actually performed matrix factorization at **only 9 anchors**, yet the full-band curve is restored smoothly!
- **Performance check** — it achieves $S_{11} = -23.24$ dB **@ 5.78 GHz**, **a broadside realized gain of 12.20 dBi** (matching the theoretical +6 dB over a single element) and **86 %** radiation efficiency.

HANDS-ON **Don't draw T-junctions by hand! 4 steps of Auto Feed + Feed Tune**

ONLY IN AETHER

1 **Select the port end faces in order**

In `F` face-selection mode, first click **the end face of the common input line**, then hold `Ctrl` and click **the feed end faces of the 4 patches** in turn from the left (5 selections in total).

2 **Run Auto Feed Network**

Open ribbon **Draw ▶ Auto Feed Network**, choose the amplitude distribution (`Uniform` or low-sidelobe `Taylor -20 dB`) and the progressive phase (e.g. `0, 90, 180, 270°`), then press **Build**, and a distribution tree including Wilkinson isolation resistors (100 Ω RLC) is laid down instantly!

3 **Tame the phase error with a single Feed Tune**

Because of T-junction parasitics and meander coupling, the initial formula synthesis shows a phase error of up to 11.7° in 3D FEM. Press ribbon **Feed Tune** to run the correction loop **just once**, and the correction-line lengths are back-calculated automatically, aligning it razor-sharp to **a maximum phase error of** 1.45°, **amplitude deviation of** 0.05 dB and **isolation of** 19.1 dB!

LAB 33-B · ZERO-RESOLVE BEAM STEERING

Difficulty ★★☆ · 8 min

Lab B: Zero seconds of FEM re-analysis! Real-time phase beam steering with `Edit Sources`

Target sample: `examples/wpt_tx_beamforming_5g8.warp`

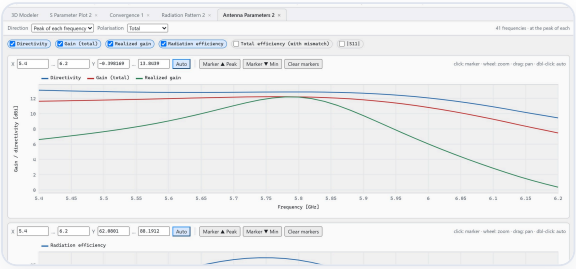


Figure 33-2 Per-frequency gain · efficiency metrics of the array antenna. Combined with Edit Sources, it compares phase-shifter scenarios instantly.

`wpt_tx_beamforming_5g8.warp` has, instead of a distribution network, an independent 50 Ω port (`P1~P4`) on each of the 4 patches. With one analysis finished, open **Results ▶ Edit Sources...** from the top menu!

1. **Enter amplitude · phase weights**
   Enter `1 W` each and phases `0°, 66°, 132°, 198°` for `P1~P4`, and press **Apply**.

2. **See the main beam move without re-analysis!**
   Switch the excitation list at the top of the far-field window to `Sources (Edit Sources)` and pick `5.825 GHz` as the frequency, and instantly, with no matrix re-solve, **the main beam swings to the $\theta = 21^\circ$ direction (13.1 dBi)**!

A hidden practical point: for a patch array on a finite ground plane, the side radiation in the horizontal plane ($\theta = 90^\circ$) differs by a whopping **15 dB** between the E-plane **(+2.8 dBi)** and the H-plane **(−11.8 dBi)**! Even a tapered feed doesn't reduce the E-plane diffracted wave, so nearby Wi-Fi devices must be placed on the array's H-plane axis to avoid interference.

LAB 33-C · 80 GHZ RADAR DETECTIVE CASE

Difficulty ★★★ · 10 min

Lab C [Detective case]: Why did the 80 GHz 2×2 radar array's broadside gain fall into a −4.8 dBi hole?

Target sample: `examples/patch_array_2x2_80g.warp` (RO3003 0.25 mm millimeter-wave board)

CASE SUMMARY **A 2×2 patch array drawn neatly with up-down symmetry, yet the wave doesn't go out broadside ($\theta = 0^\circ$) and instead splits into two lobes at $\pm 28^\circ$!**

The culprit is the geometric direction reversal at the central T-junction! If, from the central horizontal feed line, the feed lines run out in the $+y$ direction to the upper-row patches and in the $-y$ direction to the lower-row patches, then even though the T-junction voltages are in phase, the patches' feed directions face each other in space, and **the surface-current vectors of the upper and lower rows become exactly opposite (180° out of phase!)**. As a result, perfect destructive interference **(a −4.8 dBi null hole!)** is carved out broadside ($\theta = 0^\circ$).

Checking the fix: open `patch_array_2x2_80g.warp` and zoom in on the upper row's feed line! Inserting **a 1.21 mm-long U-shaped $\lambda_g/2$ phase delay line** to flip 180° once more aligns the two rows' currents in one direction, cleanly restoring **a broadside gain of +11.7 dBi** together with a 77.4–83.8 GHz wideband match (79 GHz $S_{11} = -18.1$ dB)!

34 CHAPTER

Tutorial 3 (Intermediate) · Shape Playground (rf_shapes_playground) & Mastering 1-Pass Space Mapping



Get your hands on the real-time R·L·C equivalent-circuit reader, white-handle meanders, radial stubs and Class-F stubs with automatic via shorts, all on one board, and practice the Space Mapping magic that lands a notch dead center with a single 'Solved at' number instead of 30 optimization runs!

You will learn

Decoding the RF equivalent real-time R·L·C and the formal warning

Try it

Meander white-handle dragging and the Fix length toggle

Key concepts

A 0.00 GHz-error bullseye with a single Solved at correction after converting 3 kinds of stubs

LAB 34 · RF SHAPES PLAYGROUND MASTER

Difficulty ★★☆ · 20 min

Lab prep: open a copy of `examples/rf_shapes_playground.warp`

An all-in-one practice board with a 50 Ω main line (`Line50`), 3 seed pads (`StubRadial, StubShort, StubOpen`), an independent line (`Trace`) and 2 spiral curves on a 0.813 mm RO4003C board.

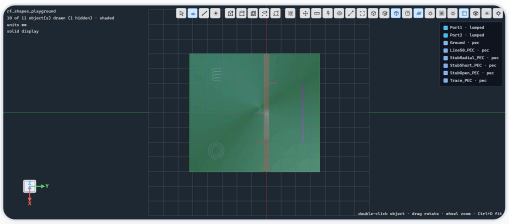


Figure 34-1 The initial rf_shapes_playground screen. Follow the 5 steps below in order and a plain through line turns into a triple harmonic trap!

34.1 Step 1 · `RF equivalent` , which reads the board below with just a click

ONLY IN AETHER

Click the center line `Line50` in the tree or viewport, and expand the `RF equivalent` section at the very bottom of the Properties pane at the lower left.

- Although you never told it the board information, it finds the `Substrate` right below ($\varepsilon_r = 3.55$, $h = 0.813$ mm) by itself and immediately calculates and shows $Z_0 \approx 50$ Ω, ε_{eff}, the electrical length (°), series $R \cdot L$ and the end C!
- Raise the number in the `Frequency` box, and **once the electrical length exceeds** 90°, a `(formal)` mark appears next to the lumped π-model — a friendly physics warning that a distributed line close to a half wavelength must no longer be replaced by single L·C part values!

34.2 Step 2 · `Meander` practice: fold and stretch by dragging the white handles

Click the straight trace `Trace` placed separately at the top, and **white round handles** appear at both ends.

1. **Length-preserving fold (`Fix length` ON, default)**
   Grab the right white handle with the mouse and drag it inward! The original total line length doesn't change by even 1 μm, while the number of zigzag turns increases in real time to fit the space (use it to cram an existing impedance-matching line inside the board edge).

2. **Phase-delay stretching (`Fix length` OFF)** UPGRADE
   Uncheck `Fix length` in Properties and enter the mm you want in `Line length`, or drag the handle. Now the footprint width stays fixed while the phase delay stretches freely!

34.3 Step 3 · One-click transformation of the 3 seed rectangles into harmonic stubs

Now pick the three small 0.5×3 mm rectangular pads attached next to `Line50` one at a time and run right-click **Stub...** (or ribbon **Modeler ▶ Stub**).

- ① `StubRadial` → `Radial` **(band** `5.5GHz - 6.1GHz` **)** — after Preview, press **Make Stub**, and the fan's apex aligns automatically with the `Line50` centerline and **the smallest fan angle covering the band (45–60°)** is chosen.
- ② `StubShort` → `Class F short stub` **(**$f_0 =$ `2.45GHz` **)** — it is converted into a $\lambda_g/4$ shorted stub to trap the even harmonic $2f_0 = 4.90$ GHz, and even **a shorting via (** `StubShort_Via` **) that pierces the board into the bottom ground is created automatically at the stub's end!**
- ③ `StubOpen` → `Class F open stub` **(**$f_0 =$ `2.45GHz` **,** `3rd` **)** — it is converted into an odd-harmonic open stub for $3f_0 = 7.35$ GHz, with the open-end fringing-extension correction applied.

> DESIGNER'S SECRET **Why does Aether EM's automatic radial stub choose only 45–60° angles instead of 90° or 145°?**
> Comparing against 7 real 3D FEM benchmarks, **45–60° fans corrected with a tapered-transmission-line cascade model are very accurate, with initial FEM errors within ±3% (only −0.9 % for this example's 45° stub!)**, whereas **90°** shifts the frequency by as much as **+15 %** due to side coupling with the main line, and **145°** merges broadly with the main line so that the stop notch disappears altogether! It's an engineering detail that recommends only verified physical regions automatically.

34.4 Step 4 · 1st FEM run → nail the 2nd FEM with `Solved at (retune)` space mapping! ONLY IN AETHER

Press `F9` to run the 1st FEM. The 2.45 GHz fundamental passes well at $S_{21} = -0.7$ dB, but because of the T-junction parasitic capacitance, the three notches land 1–4 % low, at **4.75 GHz, 5.75 GHz and 7.05 GHz** respectively. Don't just blindly run an optimizer at this point!

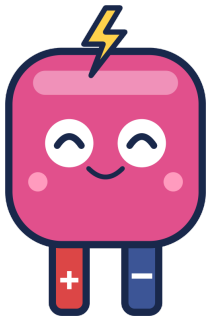
Click each stub, type the actual notch frequency you just read off the graph (`4.75GHz` , `5.75GHz` , `7.05GHz`) as-is into the `Solved at (retune)` box in the Properties pane, press `Enter`, and run `F9` just one more time!

Stub name · target role	Design target	1st FEM measured notch	Automatic shrink ratio after entering `Solved at`	2nd FEM result (just 1 re-analysis!)
StubShort ($2f_0$ short)	**4.90 GHz**	4.75 GHz (−40 dB)	$\times 0.969$ auto scale	**4.90 GHz, dead-center hit! (−48.6 dB)**
StubRadial (ISM stop)	**5.80 GHz**	5.75 GHz (−47 dB)	$\times 0.991$ auto scale	**5.80 GHz, dead-center hit! (−37.7 dB)**
StubOpen ($3f_0$ open)	**7.35 GHz**	7.05 GHz (−39 dB)	$\times 0.959$ auto scale	**7.35 GHz suppression complete (−27.4 dB)**

Bonus experiment (Step 5): select `HelixCurve` and `SpiralCurve` in the corner and apply a **Line Pattern** (width `0.3mm`). If you enter a line width excessively larger than the winding pitch, it blocks it in advance with a friendly notice, to prevent a defective self-intersecting solid (every operation can be restored instantly with `Ctrl`+`Z`!).

35 CHAPTER

Tutorial 4 (Upper-Intermediate) · 5.8 GHz WPT Rectenna + 7-Port Rectifier HB & Schematic Back-Annotation



Practice the whole chain of a wireless-power receiver (Rectenna) that receives radio waves and turns them into DC electricity! Unravel the hidden λg/4 impedance inversion of the inset feed line, then go all the way to Schottky-diode harmonic balance (HB) on a 7-port board EM and free-wiring schematic back-annotation.

You will learn

The matching secret of the 59 Ω transformer in wpt_rx_rectenna_5g8

Try it

7-port EM (K=8) + Rectifier Report triple sweep and BV breakdown diagnosis

Key concepts

SVG schematic Co-sim tuning → one-click 3D EM Lumped RLC finalize

LAB 35-A · RECTENNA IMPEDANCE INVERSION

Difficulty ★★☆ · 10 min

Lab A: Why does S11 stop at −14.6 dB when you put a 70.7 Ω transformer on a patch taken from an array?

Target sample: `examples/wpt_rx_rectenna_5g8.warp`

Open `wpt_rx_rectenna_5g8.warp` and look at the feed. A 100 Ω inset feed line goes into exactly the same patch as the Chapter 33 transmit array, but after it, instead of the commonly used 70.7 Ω transformer, sits **a 59 Ω $\lambda_g/4$ transformer**, and analyzing it gives an amazing match of $S_{11} = -29.6$ dB **at 5.825 GHz** ($Z_{\text{in}} = 46.8 - j0.4\ \Omega$, **gain 7.2 dBi, radiation efficiency 88 %**)!

The secret: the 8.8 mm-long 100 Ω inset feed line burrowing into the patch is itself almost $\lambda_g/4$ at 5.825 GHz! If the patch edge impedance R_{edge} deviates even slightly from 100 Ω, the inset line has already inverted the impedance once to $Z_1 = 100^2/R_{\text{edge}}$, so the second $\lambda_g/4$ section must be $\sqrt{(50 \cdot Z_1)} \approx 59\ \Omega$ to land exactly on 50 Ω.

LAB 35-B · 7-PORT HARMONIC BALANCE & RECTIFIER REPORT

Difficulty ★★★ · 15 min

Lab B: Follow along — 7-port rectifier EM + Schottky harmonic-balance triple sweep

Menu path: **Results ▶ Rectifier Report...** & `examples/16_rectifier_hb_5g8.py`

1 Prepare a 0.25–24 GHz wideband 7-port EM

Open Lumped Ports at 7 sites on the rectifier board — the RF input (`IN`), the matching-part pads (`CM, LM`), the DC choke (`LDC`), the diode site (`D1`), the smoothing cap (`C0`) and the load resistor (`RL`) — and run **a wideband sweep covering up to the $K = 8$th harmonic (8×3 GHz or 4×5.8 GHz)** once. (Caution: reduce it to $K = 3$ and the harmonic losses go missing, misleadingly inflating efficiency by 3–4 %p!)

2 Assign the diode & real chips, then a triple sweep

Open **Results ▶ Rectifier Report...** , assign the built-in `HSMS-286x` to `D1` (including SOT-323 parasitics $L_p = 2.0$ nH, $C_p = 0.08$ pF!) and the load `RL = 800 Ω` , then run **input power ($-10 \sim +15$ dBm) · load resistance ($100 \sim 5000\ \Omega$) · frequency sweeps**.

3 Read the power-budget bars and the `-BV` breakdown cliff!

Check the cumulative loss bars in the report on the right (reflection vs substrate heat loss vs diode R_s loss vs pure DC output) and the time waveform $v_j(t)$.

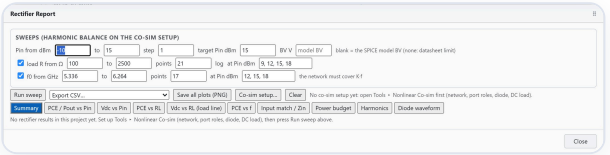


Figure 35-1 The Rectifier Report results window. It precisely catches the phenomenon where, right after efficiency peaks at 60.5 % at Pin = 12 dBm, the junction reverse voltage breaks through the HSMS-286x breakdown limit (−BV = −7 V dotted line) and efficiency plunges to 30 % at 15 dBm!

LAB 35-C · SVG CO-SIM TO 3D BACK-ANNOTATION

Difficulty ★★★ · 10 min

Lab C ONLY IN AETHER: tune in 1 second on the free-wiring schematic and back-annotate to the 3D model in one click!

Unlike other tools, there's no need to jot values on a notepad, go back to the 3D window, and delete and redraw ports one by one!

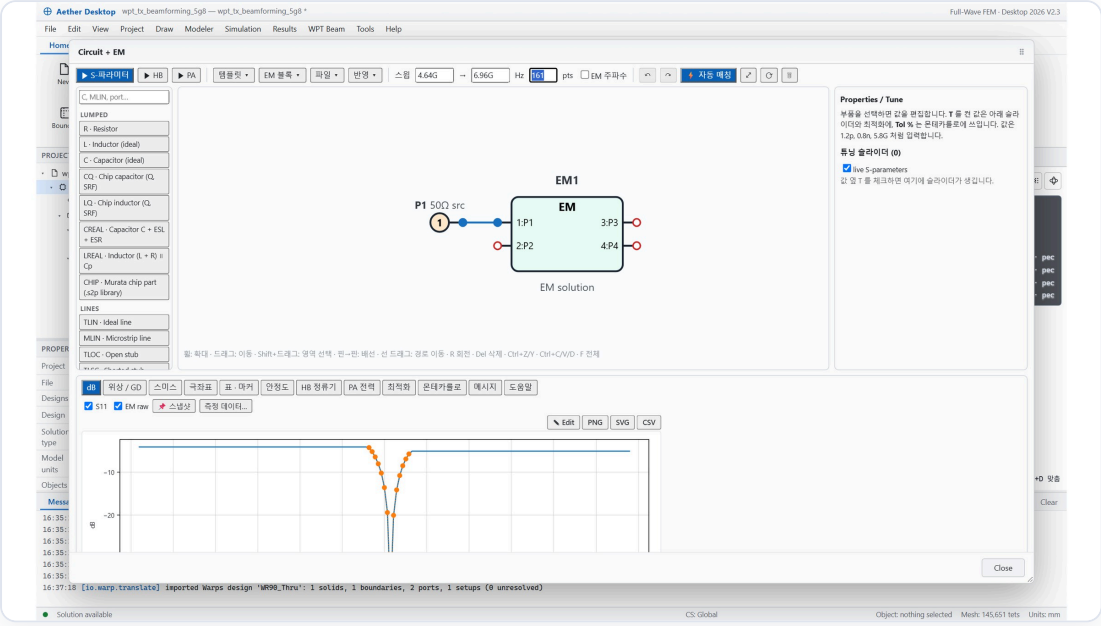


Figure 35-2 The Results ▶ Co-sim (Circuit + EM) free-wiring canvas. Wire real Murata chips (.s2p) and an NT9001 voltage-doubler Schottky pair to the 7-port EM block, and maximize rectifier efficiency (PCE %) with real-time sliders and Bayesian optimization.

1. **Open the schematic canvas and wire up parts**

   Open **Results ▶ Co-sim (Circuit + EM)...** and the current design's multiport EM block is placed automatically. From the palette on the left, drag in and connect `CHIP` (**54 Murata** `.s2p` **parts**) and high-voltage Schottkys (`SMS3923`, $BV = 46$ V, or the `NT9001` voltage-doubler pair — **200× faster convergence with the current-residual Newton engine!**).

2. **Direct Bayesian PCE optimization & E24 snap**

   In the `Optimize` tab on the right, set the goal to `Maximize rectifier efficiency PCE` and run it, then press `E24 snap` to lock to standard part values you can actually buy.

3. **The long-awaited one-click 3D back-annotation!**

   Click **Apply ▼ ▶ EM port → Lumped RLC finalize** on the top toolbar! Every L·C·R value tuned in the schematic is replaced in bulk with **real** `Lumped RLC` **boundaries** at the matching Lumped Port positions on the 3D board (single `Ctrl`+`Z` undo supported). Now one `F9` and the final 3D sign-off is done!

36 CHAPTER

Tutorial 5 (Expert Missions) · CGH40010 5.8 GHz GaN PA Tuner Adventure



Open just one project file and clear eight thrilling detective missions, and before you know it you'll have mastered everything from investigating the coarse-mesh illusion to the 4-port real-time trimmer level-up, the 400-board factory yield dice, black-anodized cooling and thermal-runaway control — V2.3's top flagship lab!

You will learn

The 4 Project Manager treasure chests and the 2f0/3f0 harmonic Q&A

Try it

L0→L4 trimmer level-up and 400-board factory tolerance (the +0.5 dB margin rule)

Key concepts

Heatsink Rca ≤ 5.95 K/W quiz · anodizing · the DE tempco thermal-runaway switch

MISSION 01 · OPEN THE CASE FILE & TREASURE MAP

Mission 1/6 · 10 min

Open the case file and search the 4 Project Manager treasure chests closely!

Target file: `examples/CGH40010_5g8_PA_Results_Thermal/pa_cgh40010_results_thermal_v2/CGH40010_5g8_PA_Results_Thermal_v2.warp`

Open the file above with **File ▶ Open Project...** (enjoy the board shape first in the 3D preview on the right of the Open dialog!). A single `.warp` file holds **1 RF electromagnetic design** (`PA_CGH40010_5g8_ClassF`) and **4 thermal designs** (`TH1` – `TH4`) together.

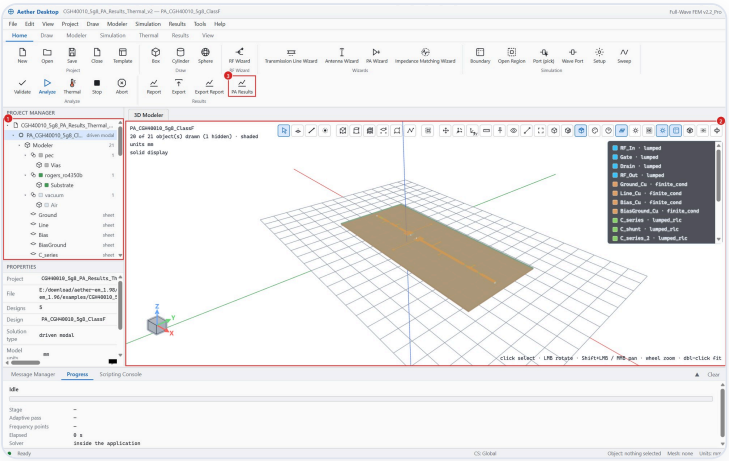


Figure 36-1 The crime scene: the 5.8 GHz CGH40010 Class-F board on a 0.508 mm RO4350B substrate. Four 50 Ω Lumped Ports — RF_In, Gate, Drain and RF_Out — are open.

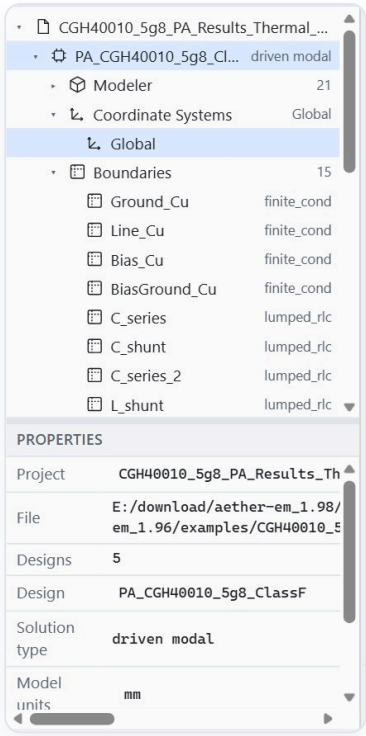


Figure 36-2 The Project Manager tree on the left: 5 multi-designs with boundaries, 4 ports and 2 sweeps.

Before opening the analysis results, double-click three settings windows in the left tree to find the 3 design devices the expert hid!

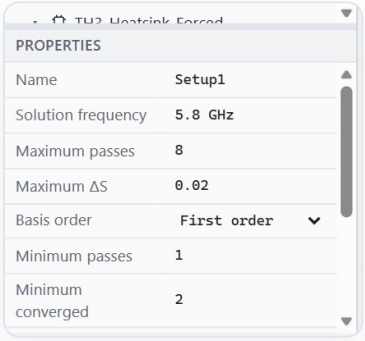


Figure 36-3 ① Setup1: 5.8 GHz, up to 8 passes, a convergence criterion of |ΔS| < 0.02 for 2 consecutive passes, second-order basis functions (shutting out the coarse 1-pass −33.7 dB illusion at the source!).

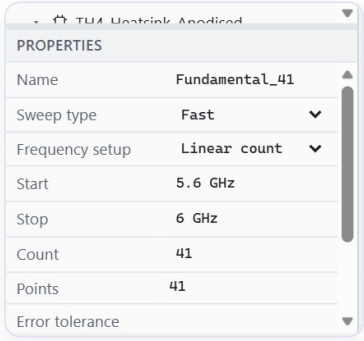


Figure 36-4 ② The double sweep: the band's 41 points run fast with Fast (5 solves), and 11.6 GHz (2f0) is extracted precisely as a single Discrete point!

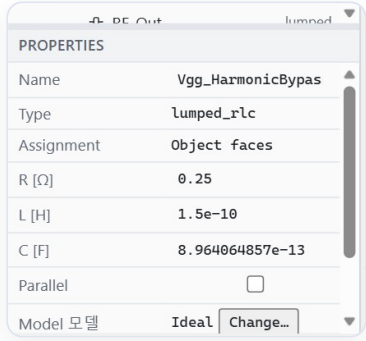


Figure 36-5 ③ C_bypass_drain: R = 0.1 Ω, L = 0.4 nH, C = 100 pF with Parallel unchecked! It mimics a real chip's series ESR+ESL+C resonance.

DETECTIVE Q&A **It's a Class-F board, so why does the harmonic sweep (`Harmonic_check`) include only $2f_0$ (11.6 GHz) and not $3f_0$ (17.4 GHz)?**

Because the package's internal capacitance is already shorting 17.4 GHz by itself! Inside the `CGH40010` package is a drain-source parasitic capacitance of about $C_{ds} \approx 1.3\ \mathrm{pF}$, whose reactance at 17.4 GHz is already only $-j7\ \Omega$. In other words, no matter how many open stubs you attach on the PCB outside the package, it is hard to create a $3f_0$ open inside the die (force a shunt C and, as Chapter 24 warns, you even ruin $2f_0$!), and for packaged GaN in this band **the real key to efficiency gains lies in protecting the $2f_0$ (11.6 GHz) short phase**.

MISSION 02 · KNOB LEVEL-UP L0 → L4 Mission 2/6 · 12 min

Open the real-time `PA Tuner` & experience the `L0 → L4` level-up, turning on one knob at a time!

Click ribbon **Home ▶ PA Results** → in `Result set` at the top left, choose `PA Tuner (live, editable)` !

ONLY IN AETHER

When the window opens, first scan in 1 minute, with the summary table below, what each of the 19 checkboxes on the left means. Every time you turn a checkbox on or off, the dashboard cards and graphs on the right rebuild instantly.

Group	Key checkbox items and how to read them in the field
1 · Small-signal & Match	**Gain / S21** (small-signal gain · band ripple), **Input S11 / Output S22** (input/output reflection), **Stability K & μ** ($\mu > 1$ across the full band means unconditionally stable!), **Smith Z_in / Z_load** (how close the drain load locus is to the Z_{opt} star)
2 · Large-signal Power	**Pout, Gain, PAE, DE vs Pin** (input-power-sweep compression curves with P_{1dB}, P_{sat} markers), **Load-pull Penalty [dB]** (the saturated-output penalty lost because the current board load strays from the optimum Z_{opt}!), **Two-tone IMD3 / ACPR** (linearity metrics)
3 · Passive PCB Audit	**PCB Insertion Loss (−10 log MAG)** (pure copper · dielectric heat loss, excluding mismatch reflection), **Gate–Drain Isolation** (reverse oscillation coupling), **2f0 / 3f0 Harmonic Z** (harmonic reflection-phase check)
4 · Tolerance & Thermal	**Monte-Carlo Yield** (400-run yield histogram with part tolerances of $\pm 1 \sim 10\%$), **Cooling Tj vs Pin & Safe Envelope** (junction-temperature curves per cooling option `TH1~TH4` , maximum survivable output, `DE tempco` thermal-runaway alarm)

Now start the trimmer L/C values on the 4 ports (`RF in` , `Gate` , `Drain` , `RF out`) from 0 (bare board, `L0`) and turn them on one step at a time to see for yourself how this amplifier wakes up!



Figure 36-6 Level L0 (all trimmers OFF, the bare-board EM as-is): worst S11 = −2.22 dB, gain ripple 6.00 dB, load penalty 4.89 dB — more than half is reflected!



Figure 36-7 Level L4 (4-port E24 trimmers ON): worst S11 = −6.01 dB (center −12.4 dB), gain 13.06 dB (ripple 1.69 dB), load penalty 0.62 dB, PAE 41.5 % achieved!

Level-up step	Trimmer knobs on	Band worst S_{11}	5.8 GHz gain (ripple)	Worst load penalty	PAE_{1dB}	Heat P_{diss} ($T_{j,TH4}$)
L0 · bare board	None (converged EM original)	−2.22 dB	9.62 dB (6.00 dB)	4.89 dB	34.5 %	4.85 W (102.8 °C)

Level-up step	Trimmer knobs on	Band worst S_{11}	5.8 GHz gain (ripple)	Worst load penalty	PAE_{1dB}	Heat P_{diss} ($T_{j,TH4}$)
L1 · first knob	`Drain` shunt C `0.75 pF`, 1 knob	−1.97 dB	9.17 dB (6.91 dB)	3.54 dB	35.5 %	5.73 W (113.1 °C)
L2 · output conquered	All 3 `Drain` elements ON	−1.91 dB	9.96 dB (5.93 dB)	**0.80 dB!**	39.1 %	8.23 W (142.3 °C)
L3 · input opened	+ 3 `RF in` + 2 `Gate`	−5.39 dB	12.85 dB (2.25 dB)	0.80 dB	41.9 %	8.19 W (141.9 °C)
L4 · complete	**All 4 ports (E24 snap done)**	**−6.01 dB**	**13.06 dB (1.69 dB)**	**0.62 dB**	**41.5 %**	**7.53 W (134.1 °C)**

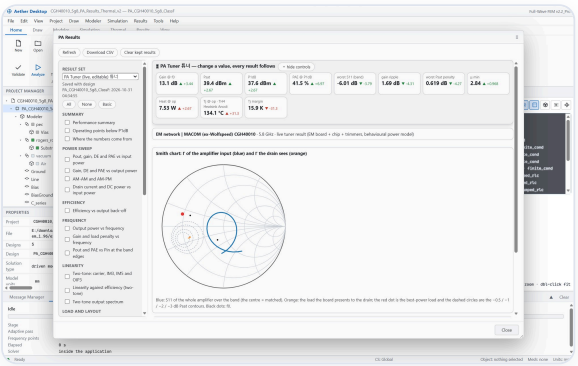


Figure 36-8 The L4 magic seen on the Smith chart: the drain load locus, scattered off in the wrong place, gathers to the dead center of the Zopt target, and the input locus slips right inside the 50 Ω circle!

Two spine-tingling physical details in the table you must not miss!

- **The textbook division of roles** — look at `L2` (tuning only the drain side)! S_{11} is still a mess at -1.91 dB, but because the drain found Z_{opt}, **the load penalty is solved in one stroke,** $4.89 \rightarrow 0.80$ dB. Then, in `L3`, matching the input · gate finally makes the gain jump by $+3$ dB!
- **Why did the chip get hotter when the tuning got better? (102.8 → 134.1 °C)** — in `L0`, half the input RF power bounced off at the board entrance, so the transistor was effectively idling ($P_{diss} = 4.85$ W)! Once the match opened up with `L4` and it started pumping out a real 8.7 W of high power, the normal operating heat of **7.53 W** was finally revealed!

MISSION 03 · AUTO-TUNE & LARGE-SIGNAL CHECK

Mission 3/6 · 8 min

Human vs robot! Press `Reset`, then the `Auto-tune` button, and inspect large-signal · linearity

Push the sliders by hand to beat the `L4` score, then take on `Auto-tune` (E24 checked)!

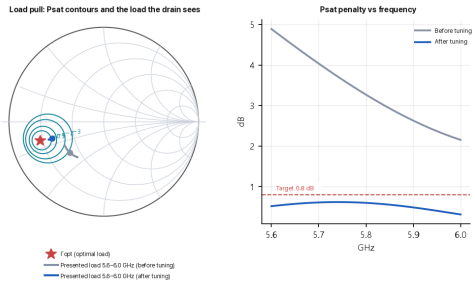


Figure 36-9 Large-signal power sweep (Pout · Gain · PAE vs Pin): PAE of 41.5 % unfolds smoothly at Psat = 39.4 dBm (8.7 W) and P1dB = 37.6 dBm.

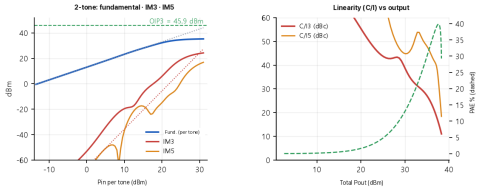


Figure 36-10 The 2-tone linearity (IMD3 · ACPR) curves: they check the back-off region and the intermodulation-distortion limit near P1dB at the same time.

MISSION 04 · THE 400-BOARD FACTORY DICE

Mission 4/6 · 8 min

The betrayal of the 400-board factory dice (48.5 % yield) and the production pro's `+0.5 dB` margin rule!

At nominal values every target is green (100 % pass), so why are half rejected once it goes to the factory?

In the tuner's `Tolerance / Yield` section, set the part tolerance to the ordinary purchase grade of `±5 %` and the number of trials to `400`, and roll! The yield of the board that passed 100 % a moment ago suddenly halves to **48.5 %** (see the Chapter 24 figure)!

- **Investigating the cause** — the `Auto-tune` robot works too honestly, exactly as told: if the target is `S11 ≤ -6.0 dB`, it stopped with its wheels hanging right on the edge of the cliff at `-6.01 dB`! Here, if the chip values wobble by just +2%, half are pushed to -5.9 dB and fail.
- **A 10-second fix exercise** — change the number in the target box to `0.5 dB` **stricter than the spec you really want** (e.g. `S11 ≤ -6.5 dB`), press Auto-tune again and roll the dice. The ±5% tolerance yield leaps from **48.5 % → over 95 %** in one go!

MISSION 05 · THERMAL QUIZ & RUNAWAY SWITCH

Mission 5/6 · 12 min

Heatsink mental-math quiz · photographing the `TH4` thermal bottleneck · triggering the thermal-runaway switch!

With midsummer air at $T_{amb} = 45\ ^\circ\mathrm{C}$, heat $P_{diss} = 7.53$ W and a package $R_{jc} = 8.0\ \mathrm{K/W}$, what does it take to keep $T_j \le 150\ ^\circ\mathrm{C}$?

No need to pull out a calculator! The allowable total temperature rise is $150 - 45 = 105$ K, of which the device package interior ($R_{jc} = 8$ K/W) already eats $8 \times 7.53 = 60.2$ K, so the case-bottom temperature must be held to 105.2 °C or below no matter what. In other words, the thermal resistance allowed for the heatsink is $R_{ca} \le \frac{105}{7.53} - 8.0 = 5.95\ \mathrm{K/W}$!

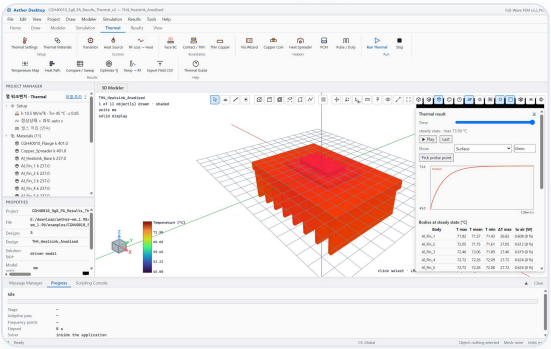


Figure 36-11 The 3D temperature field seen in the Thermal tab after double-clicking TH4_Heatsink_Anodised in the left tree: thanks to black anodizing (ε = 0.85, Rca = 3.84 K/W), a fin peak of 73.9 °C and a chip junction Tj = 134.1 °C — a pass!

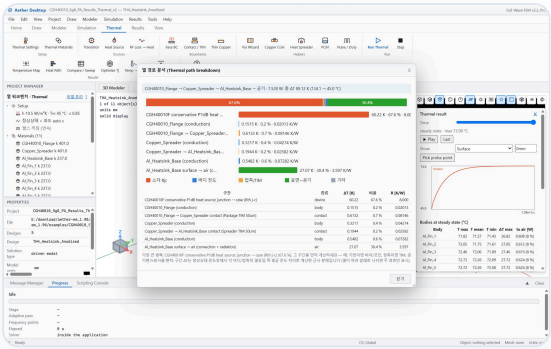


Figure 36-12 The Thermal ▶ Heat Path bottleneck breakdown bars: they prove at a glance that of the total ΔT (89.1 K), 60.2 K is the package Rjc and 28.9 K is the heatsink-to-air resistance.

A thrilling thermal-runaway experiment: go back to `4 · Heat and cooling` in `PA Results` and enter `-0.15` **[%/K]** for `DE tempco`, `-0.015` for `gain tempco` and `-0.01` for `Psat tempco` (the Chapter 31 comparison charts). The red `⚠ thermal runaway` alarm lights up on the heatsink-less `TH1` row, while the black-anodized `TH4` overcomes the efficiency-drop feedback and converges firmly at 139.1 °C!

MISSION 06 · BUILD YOUR OWN FROM PA LIBRARY

Mission 6/6 · 10 min

Graduation mission: pick a device in `PA Library` and synthesize your own new board from scratch!

You've analyzed an example someone else built; now let's create your own GaN PA project from a blank sheet.

1. **PA Library → straight to PA Wizard**

   After creating a new project with `Ctrl`+`N`, pick `CGH40010` (or the 25 W-class `CG2H40010`) in **Tools ▶ PA Library...** and press **Open in PA Wizard**.

2. **Choose a matching candidate & create the 3D board**

   Choose the target band (e.g. `5.6-6.0 GHz`) and substrate (`RO4350B 0.508 mm`), then press **Build 3D Board** on the top-ranked matching pair, and a 3D board complete with ports · bias · setup is created instantly.

3. **Clone a thermal twin**

   In the Project tree, right-click the finished design and clone it with **Duplicate Design**, rename it `TH_MySink`, then add a heatsink and a `Transistor` heat source from the **Thermal** ribbon, and the 5-design integrated package you just practiced is reborn by your own hand!

37 CHAPTER

Tutorial 6 (Flagship R&D) · CG2H40010 −33 % Miniaturization · Parasitic Audit · Metal Jig Design



Straight from a real lab's production-development notebook! The finale: shrinking the board area by 33 % while catching gate oscillation and bias leakage at once, recovering the 2.7 dB of saturated output eaten away by the package's internal Cds · Lpkg parasitics to achieve 70.5 % drain efficiency, and then bolting it onto a cutout aluminum jig.

You will learn

980 → 659 mm² (−33 %) miniaturization and gate r_feed stabilization

Try it

Recovering Psat 36.8 → 39.5 dBm with the package Cds · Lpkg parasitic audit

Key concepts

A single input-stub one-shot retune (−18.9 dB) and the cutout metal jig (Tj = 117.4 °C)

LAB 37-A · FULL-BOARD MINIATURISATION & PARASITIC AUDIT

Difficulty ★★★ · R&D practice

Lab A: Dissecting the 3 R&D design secrets of `pa_cg2h40010_5g8_full_demo.warp`

Target sample: `examples/pa_cg2h40010_5g8_full_demo.warp` (RO4350B 0.508 mm, 6-port full board)

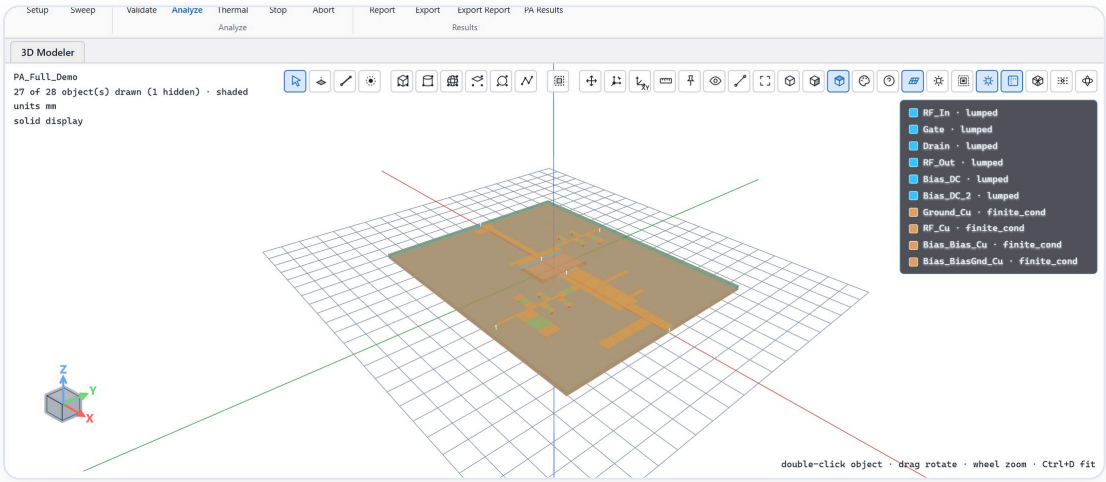


Figure 37-1 The 5.8 GHz CG2H40010 Class-F full board (659 mm²) that achieved a 33.1 % area reduction. The gate-resistor feed (upper left), the 6.8 nH lumped drain bias-T separated to the opposite side (−Y), and the intrinsic Class-F harmonic stubs gathered on one side (+Y) work in harmony.

37.1 Secret 1 · Why did isolation get better when the board shrank from 980 mm² to 659 mm² (−33.1 %)?

- **Adopting gate `r_feed` (220 Ω)** — the gate DC current is close to 0, so feeding it through a small 220 Ω series resistor instead of a huge $\lambda_g/4$ line shrank the area and, killing two birds with one stone, **wiped out the out-of-band low-frequency oscillation around 350 MHz ($\mu_{\min} = 1.18 > 1$)**!
- **Isolating the drain bias-T on the opposite side ($-Y$)** — instead of a straight $\lambda_g/4$ bias (166 mm²), it uses the 6.8 nH lumped L-C bias-T (66.8 mm²) from `Bias Designer`, but routes it out to the opposite side ($-Y$) so there is no magnetic coupling with the Class-F harmonic stubs gathered in the $+Y$ direction, **blocking parasitic coupling at $k = -40.9$ dB.**

37.2 Secret 2 ONLY IN AETHER · The package parasitic audit (Parasitic Audit) that recovered 2.7 dB of lost saturated output!

DEBUGGING IN PRACTICE **In the initial design the small-signal gain was fine, so why did the saturated output stay at `36.8 dBm`, well below the datasheet (40 dBm)?**

Opening the `Load-pull Penalty` metric in `PA Results` showed a load-mismatch penalty of a whopping **3.24 dB**! Tracing the cause revealed that **during the initial synthesis, the die current source's optimum impedance ($Z_{\text{opt,int}} \approx 15.2 + j6.8\ \Omega$) had been mistakenly entered as-is as the target outside the package leads**.

Passing it through the real `CG2H40010` package's internal $C_{\text{ds}} = 1.84$ pF and bondwire · lead inductance $L_{\text{pkg}} = 0.629$ nH, correcting to the target impedance referenced to the package terminals ($Z_{\text{opt,pkg}} \approx 8.5 + j4.2\ \Omega$) and re-synthesizing made the saturated output leap from $36.8 \rightarrow 39.5$ dBm **(8.9 W)**, and outstanding performance burst out: **a harmonic-balance drain efficiency of DE = 70.5 % (PAE = 65.2 %)**!

37.3 Secret 3 · Input S_{11} knocked off by mounting the device — fixed with a single stub in one FEM run!

The input S_{11}, perfect in the standalone passive matching network, drifted off at 5.8 GHz once the real GaN transistor was mounted — because the non-unilateral device's reverse transmission (S_{12}) let the drain load pull on the gate input impedance ($\Gamma_{\text{in}} = S_{11} + \dfrac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L}$).

Without touching the whole board again, **shortening the length of just one thing, input open stub B, from `3.77 mm → 1.47 mm`, made the full-board input reflection hit $S_{11} = -18.9$ dB @ 5.80 GHz in just 1 FEM run**!

LAB 37-B · CUT-OUT ANODISED METAL TEST JIG

Difficulty ★★★ · hardware assembly

Lab B: Final verification of the SMA end-launch + 7-fin black-anodized cutout metal jig

Target sample: `examples/pa_cg2h40010_5g8_jig.warp` (EM + Thermal multi-design)

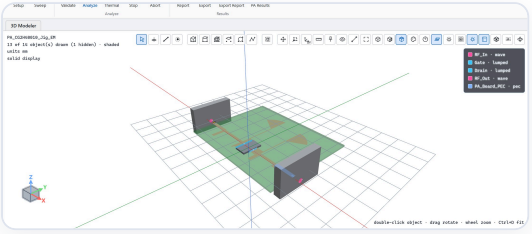


Figure 37-2 pa_cg2h40010_5g8_jig.warp: a real test jig with the GaN flange connected directly to the center pedestal of a 70×50×6 mm aluminum base, and PTFE coaxial SMA end-launch Wave Ports fastened at both ends.

Finally, open the real metal-jig file `pa_cg2h40010_5g8_jig.warp`, made for connecting this board to lab instruments (VNA/power meter), and check three hardware-finishing details!

- **SMA end-launch transition** — not a simple internal Lumped Port: a `Wave Port` is placed on a 3D SMA connector whose real PTFE-dielectric coaxial center pin rides on the microstrip pad, verifying **full-band reflection of -24.1 dB or better**.
- **Optimal natural-convection design with 6 mm fin spacing** — the spacing of the 7 black-anodized ($\varepsilon = 0.85$) cooling fins underneath is designed at 6 mm, where the air boundary layer doesn't choke (Bar-Cohen correlation $h = 10.1\ \mathrm{W/m^2K}$), achieving a fanless $R_{\mathrm{ca}} = 1.97\ \mathrm{K/W}$! Even at 45 °C midsummer heat · worst-case 7.26 W, it passes comfortably at $T_j = 117.4\ ^\circ\mathrm{C}$.
- **Reconfirming the open-top principle** — cover the $28 \times 35\ \mathrm{mm}$ pocket with a metal lid and a 6.0–6.9 GHz TE_{101} cavity resonance occurs, so the top is kept as an open `Radiation` boundary.

Part 7 masterclass wrap-up: you have now experienced at your fingertips the whole process of an industry principal engineer — ① blank-sheet coordinate modeling (Ch. 32) → ② array auto-feed · beam steering (Ch. 33) → ③ 1-pass space-mapping correction (Ch. 34) → ④ harmonic balance & schematic 3D back-annotation (Ch. 35) → ⑤ real-time PA tuning · tolerance · thermal-runaway control (Ch. 36) → ⑥ the package parasitic audit and real measurement-jig design (Ch. 37)!

PART

08

Distributed Sample Files & Script Encyclopedia
35+ Practical .warp Projects and a Python Automation Catalog

The examples/ folder in the install directory is packed with treasure-like, ready-to-run examples — from textbook exact-solution verification to ultra-thin AMC metasurfaces, 80 GHz millimeter-wave radar, high-power Gysel combiners, Wi-Fi-coexistence wireless power, the 8 standard thermal benchmarks (Th1–Th8) and the flagship GaN power amplifiers. Part 8 fully explains every sample file's design intent, verified analysis numbers, run time, and fun application points to change right after opening it.

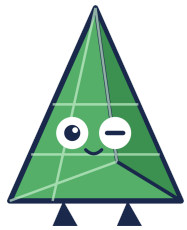


38 Catalog of 29 Samples: EM Verification · Antennas · Metasurfaces · Passive Circuits · WPT

39 Thermal Benchmarks (Th1–Th8) · High-Power PA Sample Lineage · 18 Python Scripts

38 CHAPTER

Catalog of 29 Samples: EM Verification · Antennas · Metasurfaces · Passive Circuits · WPT



Every .warp file is a finished version with shapes · materials · boundaries · ports · Setup · Sweep 100 % complete, so just open it and press F9 to get results (check the shape first in the Open dialog's 3D preview!). Pick the sample that fits your purpose and use it as the starting template for your own design.

You will learn
9 textbook theory verifications (waveguide · coax · cavity · slab)

Try it
14 practical antennas · AMC metasurface · Gysel dividers

Key concepts
6 on 5.8 GHz WPT beamforming and Wi-Fi channel 165 coexistence

38.1 The basics for seeing solver accuracy with your own eyes · 9 textbook theory-verification samples

These are the reference examples to open first when you've installed Aether EM on a new PC or want to pick up the basics of ports · eigenmodes · optimization quickly (all located at the `examples/` root).

File name (`.warp`)	Key feature · physics point	Verified FEM numbers & experiments to try	Time
wr90_waveguide	Standard WR-90 waveguide (22.86 × 10.16 mm), 2 `Wave Port` s, Interpolating sweep	TE_{10} cutoff frequency of **6.56 GHz** reproduced exactly; reflection-free X-band (8.2–12.4 GHz) transmission and $\angle S_{21}$ group-delay check	30 s
coax_line	50 Ω air coaxial line, `Wave Port` + **integration line** ($a \to b$)	TEM-mode field distribution and voltage-power-integrated characteristic impedance $Z_0 = V^2/(2P) = 50.0\ \Omega$, an exact match	20 s
parallel_plate_lumped	Parallel-plate waveguide (PMC side walls), internal `Lumped Port` , $2Z_0$ mismatched termination	Verifies decimal-place agreement with the theoretical reflection coefficient $\lvert\Gamma\rvert = \frac{2Z_0 - Z_0}{2Z_0 + Z_0} =$ **1/3** $(-9.54\ \mathrm{dB})$ at all frequencies	5 s
iris_filter	A 1-pole waveguide bandpass filter made of 2 inductive metal iris sheets	Watch the internal 2D PEC sheet boundaries and the `Fast(_ProjectedROM)` sweep restore a sharp resonant passband in seconds	1 min
cavity_eigenmode	$30 \times 15 \times 20$ mm lossless PEC rectangular cavity, **Eigenmode** 5 modes	Solved with no spurious 0 Hz modes; precise comparison of 5 eigenfrequencies with $f_{mnp} = \frac{c}{2}\sqrt{(m/a)^2 + (n/b)^2 + (p/d)^2}$	10 s
copper_cavity_eigenmode	Same-size cavity with copper walls (`Finite Conductivity`)	Computes the unloaded quality factor Q_0 from skin-resistance loss (compare directly with Pozar Eq. 6.46!)	10 s
slab_matching_parametric	Dielectric slab inside WR-90, its thickness bound to design variable `T`	Automatic search for the 10 GHz reflection-free thickness (theory 11.96 mm) with **Simulation ▶ Optimization...** or `Parameter Study`	Second s/run

File name (`.warp`)	Key feature · physics point	Verified FEM numbers & experiments to try	Time
dipole_antenna	3 GHz half-wave dipole ($0.417\lambda_0$), feed-sheet `Lumped Port`, second-order elements	$S_{11} = -16.9$ dB @ 2.95 GHz, directivity **2.19 dBi** (theory 2.15 dBi). The surface-current animation is a must-see (Ch. 32)	1 min
patch_antenna	5.8 GHz FR-4 (1.6 mm) probe-fed patch (15.7×10.94 mm, inset 2.7 mm)	$S_{11} = -20.3$ dB @ 5.75 GHz; experience the efficiency drop from FR-4 dielectric loss, then switch the material to RO4003C and compare (Ch. 32)	2 min

38.2 14 printed antennas · ultra-thin AMC metasurfaces · 80 GHz radar · passive RF circuits

These are practical 3D Full-Wave examples that include real PCB substrates, copper sheets, vias and radiation boundaries. In particular, they hold a clear answer to a question designers often hit: **"Why does a 1 mm difference in feed gap break the match?"**

File name (`.warp`)	Structure · verified numbers · designer insight	Time
metasurface_amc_dipole_5g8	**An ultra-thin artificial magnetic conductor (AMC) metasurface!** On grounded RO4003C (1.524 mm), an 18.55 mm dipole sits **just 1.5 mm** ($\lambda_0/34$, **total thickness** $\lambda_0/17$**!**) above a 5 × 5 periodic patch array (period 8.95 mm, patch 8.34 mm — a 0.927× scale tuning from the initial cell). Over an ordinary metal plate the image current would cancel it out, but thanks to the AMC's in-phase reflection it achieves $S_{11} = -21.4$ dB **(5.56–6.05 GHz)** and **a broadside gain of 8.9 dBi**!	6 min
meander_monopole_5g8 **(+ meander_monopole_2g45)**	A 4-turn meander monopole (6.48 mm wide) over a 17 mm partial ground on FR-4 1.6 mm. **The key secret:** narrow the feed gap from the ground edge to the first bend to `0.9 mm` and image coupling traps the input resistance at 8 Ω, but space it to `2.5 mm` and it hits $Z_{in} = 47 + j5\ \Omega$, $S_{11} = -24.4$ dB **@ 5.80 GHz**! (2.45 GHz version: -13.8 dB)	1 min
spiral_monopole_5g8 **(+ spiral_monopole_2g45)**	A 1.5-turn square spiral monopole (2.4 mm feed gap). Being a **low-Q wideband structure** where the partial ground plane radiates too, instead of a sharp dip it achieves **a flat** $-10 \sim -11.6$ dB **match across the whole 4.75–6.45 GHz range (1.7 GHz wide!)** (2.45 GHz version: 2.03–2.87 GHz wideband)	1 min
patch_array_1×4_5g8	RO4003C 0.813 mm 1×4 corporate-fed array. $S_{11} = -23.2$ dB, **broadside gain 12.2 dBi**, efficiency 86 % (the Ch. 33 lab version)	5 min
patch_array_2×2_80g	**An 80 GHz automotive millimeter-wave radar 2×2 array** (RO3003 0.25 mm). A **1.21 mm U-shaped** $\lambda_g/2$ **phase-correction line** on the upper row's feed line prevents the opposed-feed beam split (-4.8 dBi), achieving a **77.4–83.8 GHz match and broadside +11.7 dBi** (the Ch. 33 detective case!)	5 min
radial_stub_notch_5g8	A head-to-head between a straight $\lambda_g/4$ open stub (4.05 GHz, −44 dB) and a 60° radial stub (5.75 GHz, −40 dB) on a 50 Ω line! Compared standalone, it proves the −10 dB stopband width is 0.65 GHz for the straight stub but **1.60 GHz (2.5× wider!)** for the radial	3 min
rf_shapes_playground	All-in-one practice board for `RF equivalent` real-time R·L·C, white-handle meanders, 3 kinds of harmonic stubs & the `Solved at` 1-pass hit (Ch. 34)	4 min
pa_output_match_5g8 **(+ pa_output_match_2g45)**	Drain optimum load 12.5 Ω (port 1) → 25 Ω $\lambda_g/4$ transformer (×1.07) → 50 Ω + $\lambda_g/4$ 100 Ω bias · radial stub ($r = 6.3$ mm). $S_{11} = -25.6$ dB, $S_{21} = -0.21$ dB, verified zero parasitic resonances within 3–9 GHz!	2 min
tee_divider_2way_5g8 **tee_divider_4way_5g8**	Low-loss 1:2 and 1:4 T-junction power dividers on RT/duroid 5880 ($\varepsilon_r = 2.2$). For the 2-way divider, $S_{11} = -17.5$ dB, $S_{21} = S_{31} = -3.30$ dB (pure loss 0.29 dB, Ch. 34)	2–4 min
gysel_divider_2way_5g8 **gysel_divider_4way_5g8**	**A Gysel divider for combining high-power PAs!** Instead of Wilkinson's floating resistor, **it brings one side of the isolation resistor out to a ground via so it can be cooled through a heatsink** — a must-have topology for high power (linked to the Ch. 22 `RF Circuit Wizard`)	3–6 min

File name (`.warp`)	Structure · verified numbers · designer insight	Time
Overlap_Clear_Start_5G8 **Overlap_Clear_Result_5G8**	A before/after pair for the Chapter 10 **non-destructive copper clearance (`Clear`)** **ONLY IN AETHER**. It instantly contrasts how the area around a signal line crossing the CPWG top ground plane is automatically cut away at a $2h$ gap, resolving the short.	2 min

38.3 6 scenarios: 5.8 GHz wireless-power (WPT) beam focusing & Wi-Fi channel 165 coexistence

An original series of electromagnetic scenarios that tackles head-on how a 32 W CW wireless-power transmitter at 5.825 GHz (Wi-Fi channel 165) can **coexist** with ordinary Wi-Fi routers · laptops placed next to it!

File name (`.warp`)	Key scenario and the surprising physical truth FEM revealed!	Time
wpt_5g8_focus_demo	The Chapter 26 near-field spherical-wave focusing demo. Visually confirms the focal shift with the Fresnel number N_F and the field concentration in the beam cross-section	3 min
wpt_tx_array_5g8	A 5.825 GHz transmit sub-array on a finite ground plane ($S_{11} = -36.3$ dB, broadside 12.9 dBi, efficiency 87 %). **A decisive discovery:** only by dropping the infinite-ground assumption and solving the real finite board does the **15 dB asymmetry of horizontal ($\theta = 90^\circ$) side radiation, E-plane (+2.8 dBi) vs H-plane (−11.8 dBi)**, appear!	8 min
wpt_tx_beamforming_5g8	A phased array with 4 independently fed ports. Compares uniform (13.4 dBi) · tapered · steered ($\theta = 21^\circ$, 13.1 dBi) with `Edit Sources`, no re-analysis. Proves that even with a taper, the E-plane edge-diffracted wave (+1.9 to 3.0 dBi) doesn't shrink!	10 min
wpt_rx_rectenna_5g8	A single receive-rectenna patch (59 Ω transformer, $S_{11} = -29.6$ dB @ 5.825 GHz, gain 7.2 dBi, efficiency 88 %, Ch. 35)	3 min
wpt_wifi_coupling_5g8	Direct near-field coupling analysis between the transmit sub-array (Port 1) and a Wi-Fi half-wave dipole (Port 2) 12 cm to the side in the E-plane. Proves that **the spatial isolation between antennas is almost the same** on channel 165 (-30.1 dB) or channel 149 (-31.5 dB), and that the channel-separation benefit comes solely from receiver filter selectivity!	12 min
wpt_wifi_coupling_absorber_5g8	An experiment inserting a 20 mm lossy dielectric block ($\varepsilon_r = 2$, $tan\ \delta = 0.6$) between the board edge and the Wi-Fi antenna. A simple flat block gives **only 3.2 dB ($-30.1 \rightarrow -33.3$ dB) of improvement**, quantitatively verifying that pyramidal absorbers or $\lambda/4$ choke grooves are a must for real blocking!	12 min



A word from Aether

The results of the 5 WPT–Wi-Fi models above can also be enjoyed as **an offline Three.js interactive 3D link-budget simulator** by double-clicking `examples/wpt_wifi/index.html` to open it in a web browser! Change the distance (1–15 m) and the Wi-Fi channel and check the interference margin.

39 CHAPTER

Thermal Benchmarks (Th1–Th8) · High-Power PA Sample Lineage · 18 Python Scripts



A complete roundup of the 9 thermal-verification projects that don't touch the electromagnetic model by even a single bit (|ΔS| = 0.0), the lineage of 6 high-power GaN PA flagship samples to pick by purpose, and how to use the 18 Python scripts responsible for unattended overnight automation.

You will learn

thermal_chip_on_board for starters + the full Th1–Th8 verification number table

Try it

A guide that cleanly tells apart the 6 CG2H40010 vs CGH40010 PA samples

Key concepts

18 Python headless-API scripts and 5-line automation code

39.1 Full catalog of the 9 standard thermal benchmarks (`thermal_chip_on_board` + `Th1` ~ `Th8`) ONLY IN AETHER

Warm up with the starter `examples/thermal_chip_on_board.warp` (a 0.5 W silicon chip on FR-4 + a copper heatsink below; entering an end time of `0` auto-integrates the transient to about $5\tau \approx 1100$ s, reaching a steady state of about 80 °C, **solve time 1 second!**), then open the 8 official verification benchmarks (`Th1` – `Th8`) in the `examples/thermal/` folder in order. For all 8 models it is mathematically guaranteed that the EM S-parameter change before and after the thermal settings is **exactly** $max\ |\Delta S| = 0.0$!

File name (`examples/thermal/`)	Verified physics · key feature	Real thermal-FEM verified numbers & points to click and check
Th1_EM_loss_coupling	**RF Loss → Heat** automatic dielectric · conductor loss mapping + transient analysis	2.45 GHz 10 W waveguide dielectric heating. Auto-integrates the pure absorbed power of **6.07 W (60.7 %)**, excluding reflection · radiation → after 3 seconds of heating, the sample peak precisely reaches **42.2 °C**!
Th2_transistor_Rth_TIM	**500 W LDMOS ($P_{\text{diss}} = 220.6$ W) + copper coin + node-split solder TIM**	Left on the bare board, it would theoretically burn out at 2404 °C → with a copper coin + 50 µm SAC305 TIM + a 40 °C cold plate attached, the board is 54.7 °C and $T_j = 104.5\ ^\circ$C, tamed! The R_{jc} share (61.8 %) in `Heat Path` is a must-read.
Th3_per_face_BC_radiation_thinCu	Per-face individual convection · radiation (`Face BC`) + **thin copper (`Thin Copper`)**	A dramatic contrast: for a heater on FR-4, leaving out the lateral heat spreading of the 35 µm (1 oz) copper layer sends the temperature soaring to 595 °C, but a single `Thin Copper` checkbox makes it converge to the real board temperature of 123.5 °C!
Th4_thermal_via_wizard_compare	**Thermal Via Wizard** anisotropic homogenization (k_z, k_{xy}) comparing 4 processes	4 W QFN package: no vias **272.7 °C** → $d = 0.3/p = 1.0$ resin **100.7 °C** → $p = 0.6$ copper fill **77.4 °C** → $d = 0.5/p = 0.8$ copper fill **75.9 °C**, compared in 1 second without meshing hundreds of vias!

File name (`examples/thermal/`)	Verified physics · key feature	Real thermal-FEM verified numbers & points to click and check
Th5_enclosure_spreader_substrate_compare	**Shield-can Heat Spreader + batch sweep of 5 substrate materials** (`Compare`)	Sealed module 315.5 °C → **FR-4 150.6 °C** just by connecting the shield-can TIM! Then the substrate-swap sweep: **RO4350B 141.0 °C → alumina (Al_2O_3) 77.9 °C → aluminum nitride (AlN) 63.6 °C → metal substrate (IMS) 63.5 °C**!
Th6_PCM_pulsed_duty	**Phase-change material (PCM)** enthalpy latent heat + **pulse/duty** automatic time steps	6-second-period, 50 % duty burst heating. A paraffin latent-heat block absorbs heat in the melting range, suppressing the peak junction temperature from **114.9 °C → 103.3 °C (−11.6 K peak cut!)**!
Th7_temp_RF_backcoupling	**Temp → RF** two-way high-temperature property back-coupling closed loop	Reproduces a high-power resonator heating up and ε_r: $24.0 \to 23.43$ shifting, pushing the resonant frequency. **Fully converged at $\Delta T < 0.5$ K in just 2 EM ↔ Thermal round trips!**
Th8_auto_optimize	**Optimize Tj** monotonic-bisection automatic cooling-dimension design	On a 300 W-class package, automatically searches in just 10 thermal analyses for "the minimum copper-coin width `Coin_w` that satisfies $T_j \le 130$ °C" → derives `Coin_w = 5.83 mm` ($T_j = 129.6$ °C)!

39.2 Lineage of the 6 high-power GaN PA flagship samples, told apart at a glance

The shipped folder contains several `.warp` files related to 5.8 GHz GaN power amplifiers, so at first it's easy to get confused about which file to open. Keep each file's role and lineage straight with the table below!

File path · name	Device · ports	When should you open this file? (key purpose)
examples/pa_cg2h40010_5g8.warp	CG2H40010 · 4 ports	The cleanest basic input/output matching-network prototype. Gate $7.29 - j38.5\ \Omega$, drain $10.52 - j12.3\ \Omega$, isolation -50 dB. For checking a small-signal gain of 13.9 dB, linked with Python `14_pa_cosim_5g8.py`.
examples/pa_cg2h40010_5g8_pa_results.warp	CG2H40010 · 4 ports	The basic board above dressed with large-signal compression · load-pull `PA Results` metadata.
examples/pa_cg2h40010_5g8_full_demo.warp	CG2H40010 · 6 ports	**[Ch. 37 Lab A]** −33 % area miniaturization (659 mm²), 220 Ω gate stabilization, package parasitic audit ($P_{sat} = 39.5$ dBm, HB efficiency 70.5 %), one-shot input-stub retune (-18.9 dB) — the complete edition!
examples/pa_cg2h40010_5g8_jig.warp	CG2H40010 · jig + thermal	**[Ch. 37 Lab B]** 70×50×6 mm 7-fin black-anodized aluminum cutout jig + PTFE SMA end-launch Wave Port (-24.1 dB) + cooling ($T_j = 117.4$ °C) — the hardware-assembly version!
.../pa_cgh40010_results_thermal/ CGH40010_5g8_PA_Results_Thermal.warp	CGH40010 · v1 archive	**[Ch. 14 coarse-mesh cautionary tale!]** An archived teaching copy where a 3-point solve on a fixed 3 mm coarse grid produces the illusion of a fake $S_{11} = -33.7$ dB at 5.8 GHz.
.../pa_cgh40010_results_thermal_v2/ CGH40010_5g8_PA_Results_Thermal_v2.warp	**CGH40010 · 1 RF + 4 thermal**	**[Ch. 36 adventure master edition ★Highly recommended!]** An all-in-one teaching kit with converged EM + the real-time E24 `PA Tuner` + 400-run tolerance yield + `TH1~TH4` black anodizing · thermal runaway, all in one file!

39.3 An encyclopedia of 18 Python scripts that run dozens of models without the GUI

All of Aether EM's geometry · solver · wizard · thermal engines are open as a pure Python package (`import aether as ae`)! Here is the list of key scripts you can run instantly from a terminal with `py -3.12 examples/<script name>.py`.

Script file name	Task performed and practical use points
01_rectangular_waveguide.py ~ 04_iris_coupled_cavity.py	4 textbook starter API examples that create and analyze a waveguide · coax · parallel plate · iris filter in 20 lines of code and compare them automatically with analytic solutions
05_warps_roundtrip.py · 06_cad_import.py	Examples automating `.warp` project save · reload integrity checks and batch import of external STEP/DXF
10_dipole_antenna.py · 11_optimize_slab.py	Dipole far-field metric extraction and an automatic dielectric-slab thickness optimization loop
12_sweep_strategies.py · 13_eigenmode_cavity.py	`Discrete` vs `Interpolating` vs `Fast(_ProjectedROM)` solve-count · speed · accuracy benchmark, and cavity eigenmode · Q_0 calculation
14_pa_cosim_5g8.py · 16_rectifier_hb_5g8.py	Small-signal amplifier Co-sim combining a CG2H40010 S2P with a 4-port EM matrix, and batch runs of 7-port Schottky rectifier harmonic balance
15_wpt_wifi_fem.py	A large-scale pipeline that analyzes the 5 WPT–Wi-Fi models in sequence and automatically generates `.warp.wres` and `fem_data.js` for the web viewer
16_smart_connect_verify.py · 17_auto_feed_verify.py	Verification scripts for `Smart Connect` phase routing and `Auto Feed Network` + `Feed Tune` ($11.7^\circ \rightarrow 1.45^\circ$) automatic correction
build_examples.py · thermal/run_thermal_examples.py	Master builders that batch-generate · solve · regression-verify all electromagnetic examples and the Th1–Th8 thermal benchmarks with the `--verify` option

A headless (Headless) overnight batch-run snippet in just 5 lines

By day, polish your model comfortably in the GUI; before heading home, when you run dozens of dimension combinations, run them with a 5-line script like the one below. Open the saved `.warp.wres` result file in the GUI the next morning and pick up right where you left off with 3D fields and `AePlot` charts!

```
import aether as ae
proj = ae.Project.open("examples/patch_array_1x4_5g8.warp")
res = proj.active_design.solve_all()   # MKL PARDISO + _ProjectedROM run automatically!
print("Min S11 [dB]:", res.min_s11_db())
proj.save()
```

PART

09

Expert Appendix Emergency Troubleshooting · Menu Map · Glossary

A field first-aid manual to open right away when you run into an unexpected warning dialog or a strange graph mid-design. It brings together in one place a symptom-by-symptom cause · fix diagnostic table (covering modeling · mesh · wizards · Co-sim · thermal analysis), the shortcuts that double your working speed and a poster of all 11 menus, the solver's honest physical boundaries (supported · unsupported matrix), and a glossary of key electromagnetics · RF · WPT · heat-transfer terms.



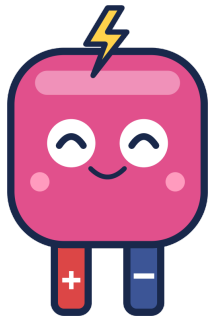
40 Symptom-Based Troubleshooting Guide

41 Complete Shortcut List and the Full Desktop 2026 V2.3 Menu Map

42 Support-Scope Matrix · Summary of Physical Limits · Key Terminology Glossary

40 CHAPTER

Symptom-Based Troubleshooting Guide



We've paired the most common baffling symptoms in the field one-to-one, from cause to immediate fix. Before you panic, look first at the yellow lines in the Message Manager at the bottom and the F5 Validation Check, and the problem is already half solved.

You will learn
Solving viewport · fast CAD import · multi-design problems

Try it
Ports · series/parallel RLC · adaptive-mesh artifacts

Key concepts
First aid for wizards (≈) · nonlinear Co-sim · thermal runaway

40.1 Display · CAD import · project management

Symptom	Common cause	Immediate fix
I opened a file but the screen is empty	Only the transparent air box is caught, or tiny parts are out of view	Run **View ▸ Display Diagnostics** (Why blank?), `Ctrl` + `D` (Fit All), or select an object in the tree and press `Ctrl` + `Shift` + `D`
An imported STEP is huge or tiny as a dot	Mismatch between the original CAD units (inch/m) and the declared units	Check the dimensions in the Import preview and set `Model units`. If already imported, reassign units with **Modeler ▸ Replace CAD Source**
I can't see the air box (`Air`)	Hidden automatically on open to keep the view clear (normal behavior)	Toggle **View ▸ Show Regions / PML**. It is only hidden on screen and is still included normally in the 3D FEM analysis (Ch. 3)
An assembly came in as a single body	Imported with `Import as single body` checked	Use per-body import (default), or run **Modeler ▸ Separate Bodies** after import

Symptom	Common cause	Immediate fix
No linewidth · meander editing for external STEP copper patterns ONLY IN AETHER	Came in as a plain solid with no parametric properties	Right-click the trace → **RF ▶ Step to RF Line...** (Ch. 12 · 36) to back-calculate the centerline · linewidth and promote it to a smart RF line, or use `Offset` in the `Faces` tab
Saved results won't open and a fingerprint warning appears	The shape · materials were modified after saving the analysis (fingerprint mismatch)	Re-analyze with `F9`, or restore from a copy of the original design in the multi-design tree

40.2 Ports · boundaries · series/parallel RLC · metal-jig resonance

Symptom	Common cause	Immediate fix
"Assignment covers 0 triangles" warning	The boundary · port sheet is slightly detached from the conductor/substrate face	In `F` face-selection mode, pick the actual contact face again, reassign it and check the port legend position
The transmission phase ($\angle S_{21}$) is flipped by 180°	The integration-line arrows of the input and output ports have opposite polarity	Right-click the port → `Reverse Polarity` or `New Line` to unify the signal→ground direction (for an 80 GHz opposed-feed array, insert a $\lambda_g/2$ U-shaped delay line, Ch. 33)
A bypass cap (`Lumped RLC`) doesn't block RF NEW V2.3	**`Parallel` checkbox turned on, so R · L · C are connected in parallel!**	A real multilayer ceramic capacitor (ESR+ESL+C) is a **series-resonant device**! Always uncheck `Parallel` (Ch. 13 · 36)
"under λ/8 ... recreate open region"	The air-box clearance is narrow relative to the lowest analysis frequency	Regenerate with `Create Open Region` based on the lowest sweep frequency (or adopt a `PML` for close-in absorption)
Wave Port Z_0 jumps abnormally	Missing integration line on a multi-conductor (MS/CPW) port, or the port window is too narrow	Specify a signal→ground integration line, widen the port window to $8 \sim 10$ times the linewidth, and check the `Port Modes` table

Symptom	Common cause	Immediate fix
The PA oscillates once placed in a metal housing/jig NEW V2.3	A TE_{101} cavity resonance occurs inside the closed metal lid	Reduce the cavity width to $a < c/(2f_{\max})$, or when analyzing the jig, remove the lid and use **an open-top air boundary** (Ch. 31 · 37)

40.3 Adaptive mesh · sweeps · optimization

Symptom	Common cause	Immediate fix
An initial 1-pass notch (−33.7 dB) disappears after convergence	**A numerical-dispersion artifact of the coarse initial mesh!**	This is normal (Ch. 14 · 36). Never trust a fixed coarse-mesh single pass; adopt results converged in $\lvert\Delta S\rvert$ for 2 or more consecutive passes
$\lvert\Delta S\rvert$ **doesn't decrease but oscillates**	The analysis frequency sits on a null, or the feed gap mesh is insufficient	Move the adaptive frequency to the passband/resonance center, and add local `Mesh Operation` refinement at ports · slots
The sweep curve shows a sawtooth ripple	A wide band was connected with sparse Discrete points	Switch to a projected reduced-order `Fast` sweep (`_ProjectedROM`) or an `Interpolating` sweep
The Far Field menu is empty	Fields not saved (especially when using `PML` alone)	Check `Save fields` in the analysis setup and re-run (Ch. 17)
Optimization (Optimize) takes too long UPGRADE	4 or more variables while using grid search/simple iteration	Switch the algorithm in **Simulation ▶ Optimization...** to `Bayesian (TPE)`, and for a single notch use the `Solved at (retune)` 1-pass correction (Ch. 15 · 34)

40.4 Auto-synthesis wizards · nonlinear Co-sim · WPT NEW V2.3

Symptom	Common cause	Immediate fix
The FEM resonance of a wizard-synthesized drawing is off by 1–4 %	The closed-form formulas (≈) don't include T-junction · corner fringing	A natural physical difference! Finish in 1–2 runs with `Solved at (retune)` for stubs (Ch. 34), `Auto-tune (FEM)` for antennas (Ch. 20) and `Feed Tune` for feed networks (Ch. 21 · 33)

Symptom	Common cause	Immediate fix
`Auto-tune` **passes 100 %, yet the ±5 % yield is 48 %**	The optimum sits right on the edge of the spec boundary (e.g. −6.01 dB)	**The production +0.5 dB margin rule:** tighten the target by 0.5 dB (e.g. −6.5 dB) and retune, and the yield instantly leaps to 95 % (Ch. 24 · 36)
The PA self-oscillates at low frequencies of a few hundred MHz	A lossless gate choke or a PDN parallel anti-resonance peak	Adopt a 220 Ω gate-resistor feed (`r_feed`) and insert a series damping resistor (R_{damp}) in `Bias Network Designer` (Ch. 23 · 37)
Harmonic efficiency dropped after `PA Tuner` **tuning**	External fundamental trimmers rotated the $2f_0/3f_0$ harmonic phase	First set the intrinsic planar harmonic traps on the board with `Class-F Auto-Stub`, then fine-trim only the fundamental (Ch. 24)
Rectifier HB efficiency halves at high input	The Schottky junction's peak reverse voltage breaks through the breakdown voltage (`-BV`)	After confirming harmonic order $K \geq 8$, switch to a high-voltage diode (e.g. SMS3923, $BV = 46$ V) and back-annotate with `Co-sim` (Ch. 25 · 35)
A red `Cavity WPT` **electric-field warning appears**	Peak electric field concentrated inside a high-Q_0 cavity (> 30 kV/m)	Lower Q_L with receiver load coupling, and operate only with a fully sealed door interlock · in unoccupied zones (Ch. 26)

40.5 Thermal workbench & cooling design UPGRADE

Symptom	Common cause	Immediate fix
`F5` `FAILED` **appears on the** `TH1~TH4` **thermal designs** NEW V2.3	The thermal-only copies are intentionally left without EM Setup/ports	**It's not a fault!** `F5` is the electromagnetic (EM) setup checker. Run thermal designs directly with the top `Thermal` **ribbon tab ▶** `Run` (Ch. 36 · 39)
The junction temperature T_j is an unrealistic $400 \sim 600\ ^\circ$C	Missing lateral heat spreading in the 35 µm copper, or a missing via/coin path	Just applying a `Thin Copper` boundary to the board surface normalizes hundreds of degrees (Ch. 28 · 39 Th3: 595 → 123.5 °C!). Check the largest bottleneck with `Heat Path`

Symptom	Common cause	Immediate fix
The mesh explodes on a thin solder/grease layer	The 50 µm TIM was modeled as a real thin 3D box	Delete the thin solid and assign a **node-split** `Contact / TIM` **boundary**, which adds no mesh at all, to the contact face (Ch. 28)
`thermal runaway` **appears in the PA cooling comparison**	Real thermal runaway caused by the efficiency temperature coefficient (`DE tempco < 0`)!	Not a numerical error but a physical thermal-runaway alarm (Ch. 31 · 36). Apply a copper coin · cutout pedestal and give the heatsink a **black-anodized** finish ($\varepsilon = 0.85$)
I packed the heatsink fins tighter, yet measurements are hotter	Air stagnation (choking) between narrow fins in natural convection	This thermal solver is a solid-conduction FEM using a surface h (no CFD, Ch. 30). In fanless natural convection, widen the fin spacing to at least $5 \sim 8\ \mathrm{mm}$

41 CHAPTER

Complete Shortcut List and the Full Desktop 2026 V2.3 Menu Map



A collection of essential shortcuts that halve your clicks once they're in your fingertips, and a full map of the 11 top menus, greatly expanded in V2.3. Every shortcut can be customized to suit your hand in Tools ▶ Keyboard Shortcuts and backed up as JSON.

You will learn
Key shortcuts for files · viewport · selection · snapping

Try it
Dedicated controls for wizards · ports · AePlot

Key concepts
Map of all 11 Desktop 2026 V2.3 menus

41.1 Essential shortcuts at a glance

Shortcut	Action
`Ctrl` + `N` / `Ctrl` + `O`	New project / open with 3D preview
`Ctrl` + `S` / `Ctrl` + `Shift` + `S`	Save / save as
`Ctrl` + `Z` / `Ctrl` + `Y`	Undo / Redo
`Ctrl` + `C` `Ctrl` + `V` / `Ctrl` + `Shift` + `V`	Copy · paste / paste and move immediately
`Ctrl` + `M` / `Del`	Precise two-point move / delete selected objects
`M`	3D distance · gap measuring ruler (Measure)
`F5`	**Validation Check (6-step pre-run EM integrity check)**
`F9`	**Analyze All (runs full adaptive FEM + sweeps)**

Shortcut · mouse	Action
`Ctrl` + `D` / `Ctrl` + `Shift` + `D`	Fit all (Fit All) / fit selected objects
`Alt` **+ click on empty space**	Snap instantly to the nearest of 8 standard views
`O` `F` `E` `V`	**Switch object · face · edge · vertex selection mode**
`B`	Cycle-select inner objects/faces hidden behind the front face
`Ctrl` **+click /** `Ctrl` **+drag**	Add to multi-selection / box-area selection
`P` / `S`	Cycle the working plane (XY · YZ · ZX) / toggle grid snapping
`Tab` → `Enter` / `Esc`	Enter exact coordinate values while drawing → confirm / cancel
`R` / `Shift` + `R` **(while placing parts)**	Rotate an SMD part 90° / reverse rotate

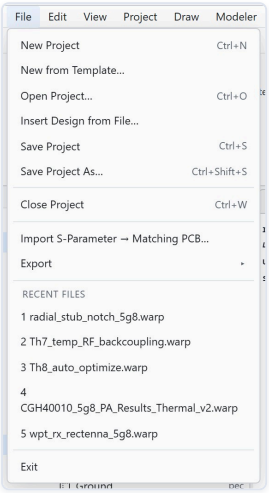
Shortcut	Action
`Shift` + `Esc`	Safe analysis stop (keeps completed pass · sweep results)

Shortcut · mouse	Action
Double-click a chart NEW V2.3	**Opens the `AePlot` modeless publishing editor (✎ Edit)**

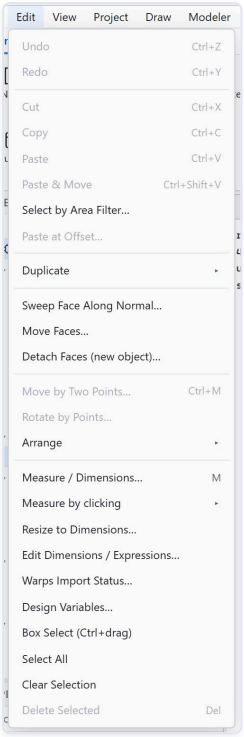
41.2 Map of all 11 top menus in Desktop 2026 V2.3 UPGRADE

In V2.3, a dedicated **WPT Beam** menu for wireless power was newly added, and the **Tools** and **Results** menus were loaded with a large set of antenna · PA · matching · filter · schematic Co-sim · 3-Line de-embedding · Vector Fit tools.

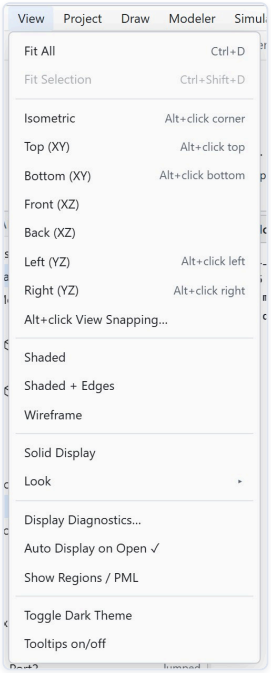
1 · File



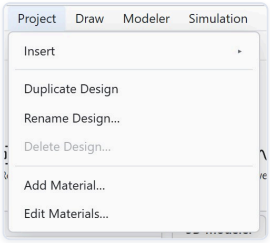
2 · Edit



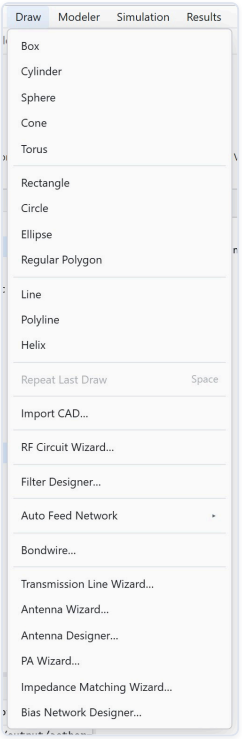
3 · View (incl. 6 Looks)



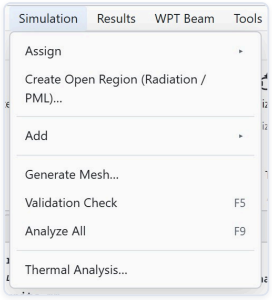
4 · Project (multi-design)



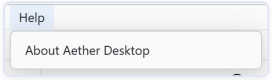
5 · Draw



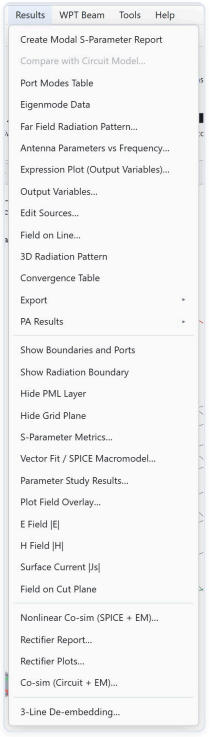
7 · Simulation

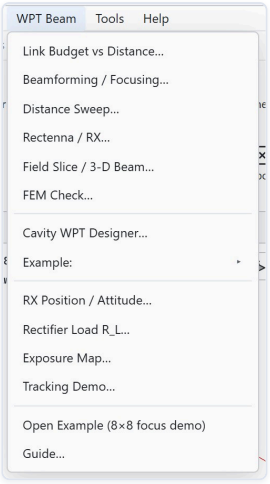


11 · Help

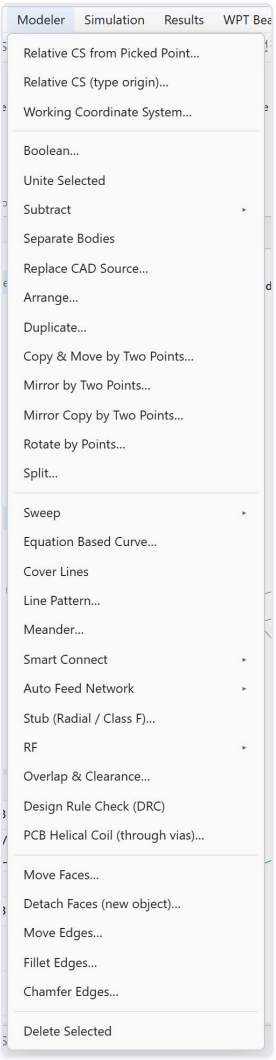


8 · Results (AePlot · PA) · 9 · WPT Beam NEW V2.3





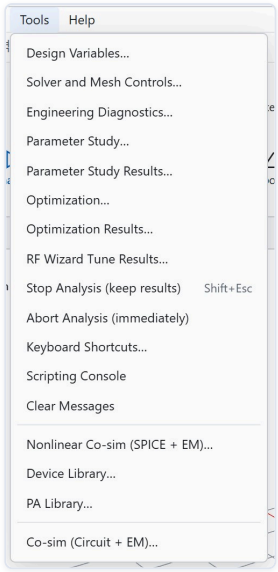
6 · Modeler (3D shapes · direct editing · RF promotion · DRC)



Modeler is the heart of CAD and RF layout.

- Coordinate systems · Booleans (Unite/Subtract/Intersect)
- Sweeps · bondwires · `Step to RF Line…`
- `Smart Connect` · `Auto Feed Network`
- Radial · butterfly · Class-F stubs and `Via Fill`
- Overlap check · `Push Neighbours` · DRC
- `Faces` direct editing (Offset / Delete & Heal)

10 · Tools (12 synthesis wizards · Co-sim · measurement correction) NEW V2.3



Tools is the headquarters of the V2.3 automatic-design ecosystem.

- `Transmission Line` · `RF Circuit` · `Filter`
- `Impedance Matching` (dual Smith · TLT)
- `Antenna Wizard` (22 arrays · metasurfaces · FPRA)
- `Antenna Designer` (Chu limit · FEM auto-tuning)
- `PA Wizard` · `PA Library` · `Bias` · `Class-F`
- `Nonlinear Co-sim` · `Co-sim (Circuit + EM)`
- `3-Line De-embed` · `Vector Fit / SPICE`

42 CHAPTER

Support-Scope Matrix · Summary of Physical Limits · Key Terminology Glossary



A good engineer knows not only what a tool can do, but exactly 'where the model's assumptions end and what it does not calculate'. Here we sum up Desktop 2026 V2.3's honest physical boundaries and key technical terms.

You will learn
An honest supported · unsupported matrix across 7 areas

Try it
6 principles for trusting analysis results

Key concepts
A glossary of essential EM · wizard · WPT · thermal terms

42.1 Desktop 2026 V2.3 support scope and honest physical boundaries

Area	Officially supported in Desktop 2026 V2.3	Physical limits · unsupported (measurement/external-tool territory)
3D EM solver	Driven Modal, Eigenmode, Nédélec 0 · 1 · Mixed/second-order elements, a-posteriori error adaptive mesh, Discrete · Interpolating · `_ProjectedROM` Fast sweeps, parallel workers, Optuna TPE optimization	Time-domain transient solvers (FDTD/FIT), pure infinite-periodic Floquet unit-cell boundaries (metasurfaces are verified with finite-aperture FEM)
Ports · boundaries	Wave Port (multimode · integration line · de-embedding), Lumped Port, Auto Port, PEC/PMC, Radiation, hexahedral PML, finite conductors with surface roughness, series · parallel Lumped RLC (including `.s2p`), symmetry planes (E/H)	Automatic labeling of dedicated differential-Terminal mode separation (calculated from ordinary multiport S-matrix combinations)
CAD · PCB	Fast binary-cached STEP/IGES/BREP/STL/OBJ, NURBS-preserving DXF, KiCad · Gerber stack-ups, `Faces` direct editing, `Step to RF Line`, JEDEC bondwires, 54 Murata `.s2p` parts	Directly opening encrypted proprietary Parasolid/ACIS binaries (converting to STEP AP214 in the original CAD is recommended)
Synthesis wizards	Transmission lines (bench copper back-calculation), 22 antennas + metasurfaces + Chu miniaturization, Smart Connect/Auto Feed, matching (p95 · TLT), filters (line compensation), the 4-step PA pipeline (competing with KiCad/ADS) + space-mapping correction	The initial synthesis (≈) is a closed-form/transmission-line approximation, so junction parasitics · surface waves · housing coupling must always be finished in 3D FEM
Nonlinear · circuit	Multiport EM + SPICE Schottky-diode harmonic balance (HB, 200× faster for voltage doublers), free-wiring SVG schematic `Co-sim`, the real-time 0.1-second `PA Tuner` (E24 snap), one-click Lumped RLC back-annotation	Direct multitone HB integration of full transistor-waveform physical models (Angelov/EEHEMT) (the PA tuner is based on measured S2P · load-pull · behavioral compression models)
WPT · cavity	Goubau beam collection efficiency (BCE), Fresnel near-field focal shift (N_F), retrodirective pilot phase conjugation, the $10\ \mathrm{W/m^2}$ human safety line, 433 MHz `Cavity WPT` mode · dielectric-breakdown diagnosis	Certified 3D voxel analysis of local SAR inside living tissue (a conservative power-density safety radius guide is provided)
Thermal · cooling	Independent solid-conduction 3D FEM ($\lvert\Delta S\rvert = 0$), steady state · automatic 5τ transient, Transistor · `RF Loss→Heat`, node-split TIM, `Thin Copper`, thermal vias · copper coins · heatsinks · PCM · pulse, `Optimize Tj`, `Temp→RF`, anodizing (ε) · thermal-runaway diagnosis	Navier–Stokes fluid dynamics (CFD; air stagnation between narrow fins needs the user's judgment of h), face-to-face view-factor mutual radiation, nonlinear $k(T)$

42.2 6 engineer habits that make simulation results 100 % your own

01

Don't trust a coarse single pass

First check that $|\Delta S|$ in the convergence table has settled below the criterion for consecutive passes.

02

The wizard (≈) is the starting line

Close the loop with FEM using `Solved at` · `Auto-tune`.

03

Look at efficiency beyond S11

Look at radiation efficiency (η), intrinsic harmonic impedance and heat loss together.

04

Leave a +0.5 dB production margin

To survive the 400-board tolerance dice, leave headroom inside the spec line.

05

Tie temperature and RF together

For high-power circuits, check `DE tempco` thermal runaway and high-temperature drift as well.

06

Finish with bench measurement

Match model and hardware with 3-Line de-embedding and copper-tape back-calculation.

42.3 Key terminology glossary: electromagnetics · wizards · WPT · thermal analysis

Term	Clear practical definition
Nédélec vector elements	The standard 3D EM finite element that places tangential electric-field degrees of freedom on tetrahedron edges rather than nodes, eliminating interface discontinuities and spurious solutions (Spurious modes) at the source
`_ProjectedROM`	A reduced-order fast sweep that projects the full FEM matrix onto the high-accuracy solution space solved at a few anchor frequencies, restoring the response at hundreds of frequencies in seconds
Space Mapping	A correction technique that back-calculates only the frequency/impedance deviation between a fast closed-form wizard model and a slow but accurate 3D FEM model, hitting the target in just 1–2 iterations (`Solved at`)
Chu Limit	The fundamental physical law that as the minimum sphere enclosing an antenna (ka) shrinks, the minimum achievable resonant Q soars as $1/(ka)^3$, limiting the bandwidth · efficiency product
Intrinsic drain plane (Intrinsic Plane)	The location of the actual semiconductor die current source with the transistor package lead · bondwire parasitics (L_{pkg}, C_{ds}) stripped away. The true reference plane where the Class-F $2f_0$ short/$3f_0$ open must form
MAG-based board loss	The $-10\,log_{10}(\text{MAG})$ metric that mathematically separates mismatch reflection from the simple $\lvert S_{21}\rvert$ of an impedance-transforming matching network, isolating only the pure copper · dielectric heat-dissipation loss
Harmonic balance (HB)	A steady-state method that keeps nonlinear devices (diodes, etc.) as time-domain waveforms and the linear EM board as a frequency-domain harmonic matrix, and solves so that the Kirchhoff current error becomes 0
3-Line de-embedding	A non-standard calibration technique that extracts the error boxes of connector · launch fixtures from measurements of just three uniform transmission lines of different lengths, isolating the pure DUT S-parameters
Vector Fitting & passivity	A technique that approximates EM S-parameters as a rational sum of poles and residues to turn them into a SPICE equivalent circuit, while correcting it so it never creates energy by itself at any frequency ($\lVert S\rVert_2 \le 1$)
Goubau τ · BCE	The wireless-power diffraction-limit parameter (τ) set by the transmit/receive aperture sizes and the distance, and the theoretical maximum beam collection efficiency (Beam Collection Efficiency)
Node-split TIM · thin copper	Boundary techniques that accurately model the through-thickness temperature step of tens-of-μm solder/thermal pads (node splitting) and the lateral heat spreading of a 35 μm copper layer (tangential conduction) without thin 3D meshes
Black anodizing (ε)	A technique that anodizes the surface of an aluminum heatsink to raise its infrared emissivity ε from 0.10 → 0.85, maximizing Stefan–Boltzmann radiative cooling 5× even without a fan

Term	Clear practical definition
Thermal Runaway	A positive-feedback phenomenon in which a temperature rise lowers PA efficiency (`DE tempco < 0`), and the extra lost heat pushes the temperature up again, until it runs away all the way to the device-destruction temperature

PART 10

10

Revision Supplement
2026-11 Updates & Results · Export · AI



This part gathers in one place the features that entered the tool after the main 9 parts were written, along with result reading · export · second-phase wireless power · AI integration, which were missing until now. Every number comes from real analyses and real screens.

43 Setup Advisor, checked before analysis, and the new speed defaults

45 Reading current · E · H · radiation from one dipole

47 AI agents and Physical AI integration

49 New modeling features

+ Field cheat sheet

44 Results to files: Export in full

46 Phase-2 wireless power: tracking · exposure · pose · rectifier · resonator

48 New screen · project · data features

50 New PA · rectifier · thermal · antenna-wizard features

11 PART 11 Complete menu · ribbon reference

10.0 How to read this part

The main text through Part 9 is left as it is, and the new content is gathered in this part. The table below shows 'which supplement chapter to read next while reading which main chapter'.

Main chapter	Supplement chapter to read next	What it adds
Ch. 14 Solution Setup	Ch. 43 Setup Advisor	Pre-analysis settings check, Fast-sweep default
Ch. 15 Check · run	Ch. 43	Apply / Ignore flow, measured evidence
Ch. 16–17 Reading results	Ch. 45 Four dipole results	S11 · Smith · current · E · H · radiation in one example
Ch. 18 Sharing	Ch. 44 Export in full	3D viewer, report, Paper, DXF, Touchstone, CSV
Ch. 26 WPT Beam	Ch. 46 Phase-2 WPT features	Moving-RX tracking, exposure map, pose, R_L, resonator
Ch. 39 Python scripts	Ch. 47 AI · Physical AI	Agent loop, verified CLI output
Ch. 3 · 4 · 18 Screen · files · plots	Ch. 48 Screen · project · data	Look, multiple designs, plot editor, macromodel
Ch. 8 · 10 · 11 Modeler · RF tools	Ch. 49 New modeling features	Bondwire, real chip parts, Via Fill, stubs
Ch. 20 · 23 · 25 · 27	Ch. 50 PA · rectifier · thermal · antenna	PA Tuner, rectifier report, 22 antenna families
Full menu · ribbon	PART 11 Reference	Every item on screen and its shortcut

10.1 Revision summary: what's new NEW

Area	Additions · changes	Ch.
Analysis setup	Setup Advisor (Simulation menu); new sweeps default to Fast; wave-port low-rank ON by default	43
Export	three.js 3D viewer (complex E · H · Js, arbitrary cut planes · probes), HTML · PDF report, IEEE paper draft, DXF 2D · 3D	44
Reading results	Smith chart markers, current · E · H phase animation, 3D gain pattern	45
Wireless power	Exposure Map, Tracking Demo, RX Position / Attitude, Rectifier Load R_L, Resonator WPT, Cavity Resonator Designer	46
Automation	aether new · solve · validate · info, Python API, text .warp workflow	47
Screen · project	6 View ▶ Looks, multiple designs in one project, plot editor, parallel sweep, vector-fitting macromodel, Bayesian optimization	48
Modeling	Bondwire, real chip parts (.s2p), Via Fill, C/L stub shapes, SMD @ Point, Meander length release, Open Region	49
PA · thermal · antenna	PA Tuner (real-time), rectifier report, thermal workbench, 22 antenna families and auto-tuning	50
Terminology	Basis-order names changed (Zero / First / Mixed), default First order	48.9
Figures	GUI figures in the main text replaced with the latest screens; 3 broken figures (19-2 · 20-1 · 26-1) restored	All



A word from Aether

Read the 'measured' and 'estimated' labels next to the numbers separately. In this part's tables, **measured** means a value actually run, and **design calculation** means a value obtained from a model formula.

43 CHAPTER

Setup Advisor, Checked Before Analysis, and the New Speed Defaults



A helper that reads the model before you press the analysis button and suggests settings matched to your accuracy target, **with evidence**. It changes nothing automatically and applies only what you pick.

You will learn
Where to open Setup Advisor and the order to read it in

Try it
Check your model with Simulation ▶ Setup Advisor...

Key concepts
Accuracy target vs speed, measured · estimated · pending labels

43.1 What it reads and what it suggests NEW V2.3

Open **Simulation ▶ Setup Advisor...** . It also appears automatically before you start an analysis (Analyze Start), with a model summary at the top and a list of recommendations below.

Item read	Example: 5.8 GHz beamforming example
Frequency	5.725 – 5.925 GHz
Model size	174.63 × 65.52 × 26.55 mm (3.45 λ0)
Substrate	εr 3.55, h 0.813 mm
Copper · Vias	Sheets 0 · vias 0
Ports	4 (wave 0), radiation boundary present → sharp resonances possible
Memory	10.6 GiB free. Checks in advance whether the analysis will fit

The 'Explanation' column tells you what that value means for the analysis (e.g. λ0, λg from the effective permittivity, h/λg). When the model changes, the values change too.



Figure 43-1 Setup Advisor. Top: accuracy target and model summary; middle: measured table by order; bottom: recommendation list (Apply all · Apply selected · Ignore).

43.2 Reading the accuracy target and the recommendations

The helper's criteria are **S21 phase within 1° of the converged true value**, and **a fast sweep within 0.5 dB · 2° of a discrete sweep on the same mesh**. Recommendations are applied only when you press Apply, and Ignore changes no settings at all. Expand the evidence with **Evidence ▸ show** in the window.

MEASURED
Numbers that came out of an actual run. The most trustworthy.

ESTIMATED · PENDING
Estimated means an extrapolated value; pending means the feature exists but hasn't been verified against the target yet, so use it only when needed.

Measured evidence for choosing the order (same accuracy target)

Model	Order	Time	Memory	Phase error
Microstrip 15 mm	First (p1)	122.8 s	2.68 GiB	0.8°
	Second (p2)	47.8 s	1.88 GiB	0.5°
	Mixed	80.2 s	2.54 GiB	0.1°
Microstrip 50 mm	First (p1)	91.7 s	2.94 GiB	1.1°
	Second (p2)	60.2 s	2.22 GiB	0.6°
	Mixed	81.4 s	2.51 GiB	0.2°

Recommendations from the beamforming example (first 2 of 4)

- **Adaptive convergence** estimated: ΔS 0.03 · 8 passes → ΔS 0.02 · 10 passes or more. It explains that for a patch · antenna model with a radiation boundary, the reflection |S11| and resonant frequency have already converged at ΔS 0.02, and forcing 0.003 only adds passes with almost the same result.
- **Refinement marking** measured: fraction → Dörfler (θ 0.6). It refines only the elements with large error, so the tet growth per pass is small; on a solid model it went from 208.6 s → 96.7 s.

Scroll the window down to see the remaining recommendations. The number and content of the recommendations differ from model to model.

HOW TO **5 steps**

1. After opening the model, open `Simulation ▶ Setup Advisor…`.
2. Check that the model table at the top matches your model (frequency, size, number of ports).
3. For each recommendation, read its **measured** label and evidence.
4. Check only the ones you'll use and press **Apply selected**. To use them all, Apply all.
5. Run Analyze. You can check and change the applied values in the Setup window.



Wiz's warning
Some **pending** recommendations were found in verification to give 'no benefit at the same accuracy' (e.g. via lowpoly). Read the evidence and turn them on only when needed.

43.3 The newly changed speed defaults 2026-11-05

Accuracy was left unchanged (|ΔS| < 1e-3 on the same mesh as the criterion; measured at the 1e-13 level) and only the slow parts were fixed. Every one can be turned off with a setting or an environment variable.

Item	Default	Explanation · how to turn it off
Fast sweep	Default for new sweeps	Newly created sweeps are Fast and port interpolation (port_interp) is on. Turn it off with `AETHER_PORT_INTERP=0`. Already-saved sweeps are not changed.
Wave-port low-rank	ON	Uses Woodbury low-rank updates. Large port faces are solved with sparse shift-invert. `AETHER_PORT_LOWRANK=0`
Mixed-order rule	opt-in	`AETHER_MIXED_RULE=band2`: second order near metal · ports, first order outside. In measurements it was no better than the default field rule.
Parallel · batched assembly	opt-in	`AETHER_ASSEMBLY_WORKERS=N`: parallel assembly cuts 38–48 %, but for small models the total time is about the same. `AETHER_FAST_ASSEMBLY=1`: batched assembly makes the assembly stage 2–2.4× faster.
Substrate z-stretch mesh · copper union · port imprint	opt-in / auto	The 2-D union of copper sheets is used only when shapely is present; otherwise it runs with the existing OCC method.

Bandpass filter total time	PA example total time	|ΔS| difference vs previous version
53.0 → 25.4 s (2.1×)	**41.9 → 33.9 s (1.24×)**	**≈ 1e-14**

Source: measurements in the speed-improvement document (2026-11-01, 4 threads, alternating runs with the previous version on the same PC). Results vary by model and PC; the number of adaptive passes · mesh · full solves was identical to the previous version.

HOW TO **After applying the update**

1. Hard-refresh the browser with `Ctrl+F5`.
2. Create a new sweep and check that Fast is set by default.
3. Sweeps in earlier projects stay as they were, so switch them to Fast and re-solve if needed.

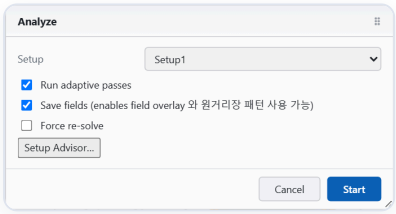


Figure 43-2 The Analyze dialog.

Press **Analyze All (F9)** and this window appears first. Choose the **Setup**, decide on **Run adaptive passes**, **Save fields** (needed for field overlays and far-field patterns) and **Force re-solve** (solve again even if a saved solution exists), then press **Start**. The **Setup Advisor...** button opens the check window from here too, and after Start, Setup Advisor appears once if there are recommendations (Apply all · Apply selected · Ignore).



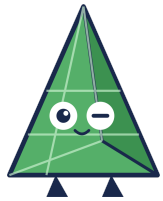
Mesh's tip

After changing speed options, overlay one or two S11 points from the same model on the previous result. It's the quickest way to confirm by eye that the accuracy is the same.

44 CHAPTER

Results to Files: Export in Full

Analysis results don't end on the screen. You can take them as they are into a 3D viewer, reports, a paper draft, drawings and standard data files.



You will learn
Export formats and where the menus are

Try it
Make a shareable HTML with File ▶ Export 3D Viewer

Key concepts
Can the recipient open it without Aether?

44.1 Export map UPGRADE

Format	Menu	What it holds · how to open
three.js 3D viewer .html	File ▶ Export 3D Viewer (three.js)...	Model and results. Opens in a browser; needs no Aether · Python · network
PDF report	File ▶ Export Report...	Model views, materials · boundaries · ports · settings, S-parameters, convergence history, field · thermal figures
HTML report	aether solve ... --out NAME	One sheet of summary tiles and tables. Generated in one go together with S-parameters · CSV
Touchstone .sNp	Results ▶ Export S-parameters...	Port names are included as comments (Port[1] = p1)
CSV	CSV button in a graph window · NAME_sparams.csv	dB and phase columns per frequency
IEEE paper draft	File ▶ Export ▶ Paper...	IEEEtran two-column .tex + figs/ + .bib, plus .docx · .pdf on request
DXF drawing	File ▶ Export ▶ DXF Drawing...	2D layout or 3D surfaces, units mm
CAD · solution data	Export CAD Geometry... · Export Solution Data...	Shapes as CAD files, solutions as data files



A word from Aether
When sending to a customer or colleague, **a single 3D viewer .html** is enough. Without installing anything, the recipient can move the cut plane and rotate the phase.

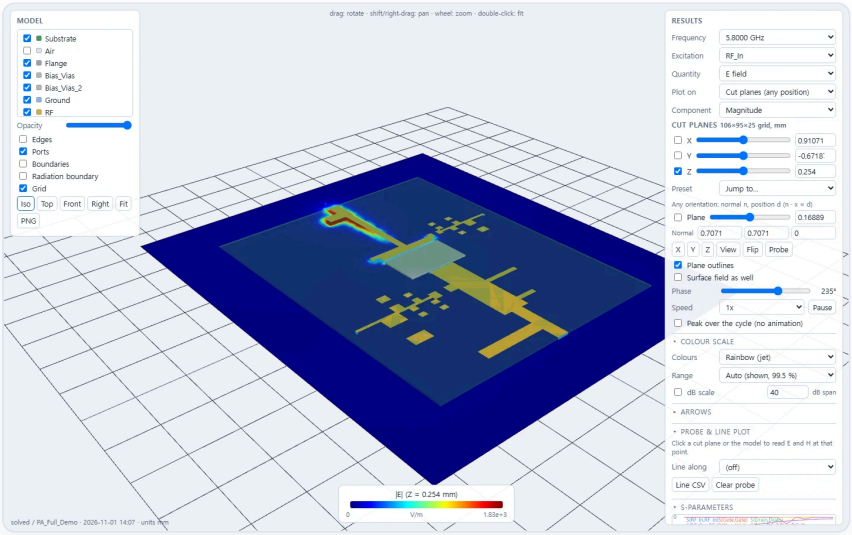


Figure 44-1 A three.js viewer actually exported by the tool, opened in a browser (about 6 MB, 0 external requests). Turn off Edges and the mesh lines disappear, making the field colors clearer.

44.2 Looking inside the three.js 3D viewer

The viewer file holds not only the model's triangles, colors and transparency, port · boundary faces and edges, but also the saved frequencies and, per excitation, **the complex E · H · surface current** and the complex far field. The fields are stored on a grid refined at each boundary, so you can make a cut plane at any position.

HOW TO VIEW

- X · Y · Z cut-plane sliders, one arbitrary-normal cut plane
- Phase slider and speed (1x), Pause, one-cycle peak
- Probe: click a point to read E · H values, Line CSV

VIEW OPTIONS

- Color range Auto (99.5 %), dB scale, colormap
- Edges · Ports · Boundaries · Grid display, save PNG
- Iso · Top · Front · Right views, transparency

How it stays small

Every binary array is compressed with zlib, and identical arrays are stored only once. Complex fields are stored as a 10-bit log magnitude (80 dB, 0.08 dB steps) and an 8-bit phase (1.4°) with delta encoding, and three.js itself is embedded compressed.

HOW TO **Making a viewer to share**

1. Turn on **Save fields** when analyzing and run Analyze.
2. Choose `File ▶ Export 3D Viewer (three.js)…` and set the file name.
3. Double-click the resulting .html to check it in a browser.
4. Before sending, set the cut plane (Z slider) where rotating the phase will show one cycle.



A word from Wiz

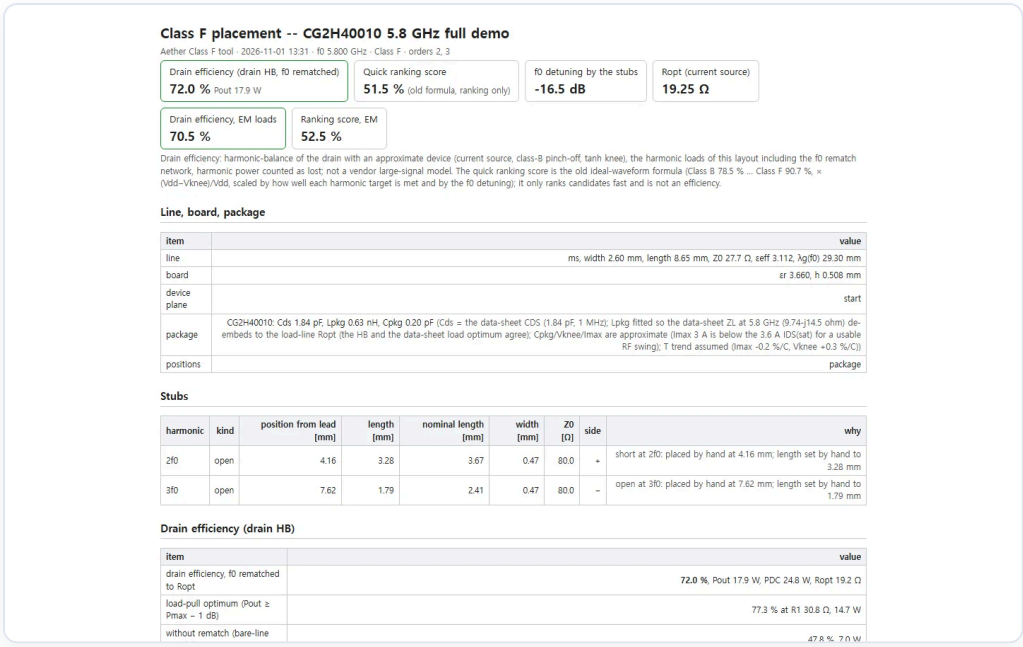
The viewer background follows the recipient's system color scheme. For images to put in documents, turn off Edges in the light color scheme and save as PNG for a clean result.

44.3 Taking the numbers: Touchstone · CSV

```
! Touchstone file written by Aether-EM
! 2-port S-parameters, 10 frequency points
! Port[1] = p1
! Port[2] = p2
# GHz S RI R 37.673
1 -2.688e-09 -6.080e-09 0.91343 -0.40700 0.91343 -0.40700 ...
```

Port names are included as comments, so other tools and Co-sim read the port mapping as-is. The CSV comes out with columns `Freq[Hz], dB(S11), ang(S11)[deg], …`.

44.4 Reports · paper draft · drawings



Class F placement -- CG2H40010 5.8 GHz full demo

Aether Class F tool · 2026-11-01 13:31 · f0 5.800 GHz · Class F · orders 2, 3

Drain efficiency (drain HB, f0 rematched)	Quick ranking score	f0 detuning by the stubs	Ropt (current source)
72.0 % Pout 17.9 W	51.5 % (old formula, ranking only)	-16.5 dB	19.25 Ω

Drain efficiency, EM loads	Ranking score, EM
70.5 %	52.5 %

Drain efficiency: harmonic-balance of the drain with an approximate device (current source, class-B pinch-off, tanh knee), the harmonic loads of this layout including the f0 rematch network; harmonic power counted as lost; not a vendor large-signal model. The quick ranking score is the old ideal-waveform formula (Class B 78.5 % ... Class F 90.7 %, × (Vdd−Vknee)/Vdd, scaled by how well each harmonic target is met and by the f0 detuning); it only ranks candidates fast and is not an efficiency.

Line, board, package

item	value
line	ms, width 2.60 mm, length 8.65 mm, Z0 27.7 Ω, εeff 3.112, λg(f0) 29.30 mm
board	εr 3.660, h 0.508 mm
device plane	start
package	CG2H40010: Cds 1.84 pF, Lpkg 0.63 nH, Cpkg 0.20 pF (Cds = the data-sheet CDS (1.84 pF, 1 MHz); Lpkg fitted so the data-sheet ZL at 5.8 GHz (9.74-j14.5 ohm) de-embeds to the load-line Ropt (the HB and the data-sheet load optimum agree); Cpkg/Vknee/Imax are approximate (Imax 3 A is below the 3.6 A IDS(sat) for a usable RF swing); T trend assumed (Imax -0.2 %/C, Vknee +0.3 %/C))
positions	package

Stubs

harmonic	kind	position from lead [mm]	length [mm]	nominal length [mm]	width [mm]	Z0 [Ω]	side	why
2f0	open	4.16	3.28	3.67	0.47	80.0	+	short at 2f0: placed by hand at 4.16 mm; length set by hand to 3.28 mm
3f0	open	7.62	1.79	2.41	0.47	80.0	–	open at 3f0: placed by hand at 7.62 mm; length set by hand to 1.79 mm

Drain efficiency (drain HB)

item	value
drain efficiency, f0 rematched to Ropt	72.0 %, Pout 17.9 W, PDC 24.8 W, Ropt 19.2 Ω
load-pull optimum (Pout ≥ Pmax − 1 dB)	77.3 % at R1 30.8 Ω, 14.7 W
without rematch (bare-line	47.8 %, 7.0 W

Figure 44-2 An example HTML report exported by the tool (Class F placement report). Every value in the summary tiles and tables is calculated from the solution.

Format	Things to know
PDF report	Creates a multi-page PDF with views of the model from several angles, objects · materials · boundaries · ports · analysis settings, S-parameters (dB · phase · Smith), a resonance table, convergence history and field · thermal figures. It embeds a Korean font (NanumGothic), so it looks the same wherever it's opened.
IEEE paper draft	Every number in the body comes from the design · solution · built-in analysis models. Contributions · related work · discussion are left blank as `[TODO: …]`, and references are taken only from the list built into the app. It's a draft, so a person has to fill it in.
DXF drawing	2D has closed outlines (LWPOLYLINE, arcs as bulge, circles as CIRCLE) and optional HATCH; 3D has 3DFACE surfaces and CAD edge polylines. Layers are by object · material · z plane.

HOW TO **Making a paper draft**

1. Keep the analyzed design open.
2. In `File ▶ Export ▶ Paper…`, choose whether you need .docx · .pdf.
3. Open the resulting .tex and figs/ and fill in the `[TODO]` paragraphs yourself.
4. If pdflatex is available it makes the PDF; otherwise the built-in ReportLab two-column renderer does.



Porty's check

First check **the units and layer rules** required by the manufacturer receiving the drawing. This tool's DXF is in mm, and the layers are chosen by object · material · z plane.

44.5 The export dialogs at a glance

Each item under **File ▸ Export** (or Results ▶ Export) opens a short settings window. The 3D viewer opens a file window to choose the save location and name (.html), and **Save fields** must be on during the analysis for fields to be included. The others are as follows.

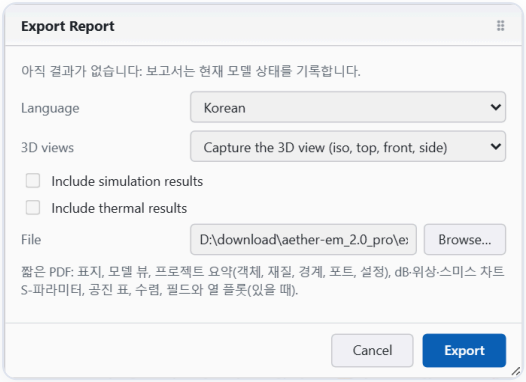


Figure 44-3 Export Report. Language (Korean / English), 3D views (isometric · top · front · side, 4 directions), Include simulation results · Include thermal results, File. Without analysis results it records only the current state.

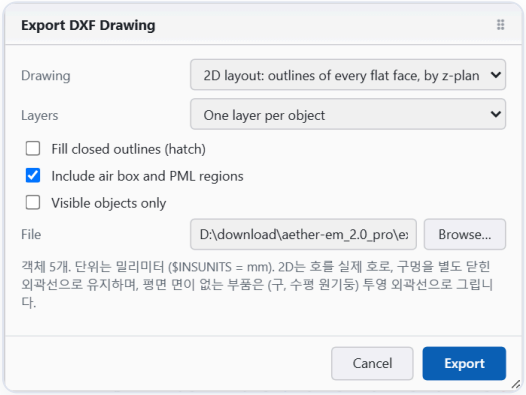


Figure 44-5 Export DXF Drawing. Drawing (2D layout of planar shapes by z plane), Layers (one layer per object), Fill closed outlines (hatch), Include air box and PML regions, Visible objects only. Units are mm.

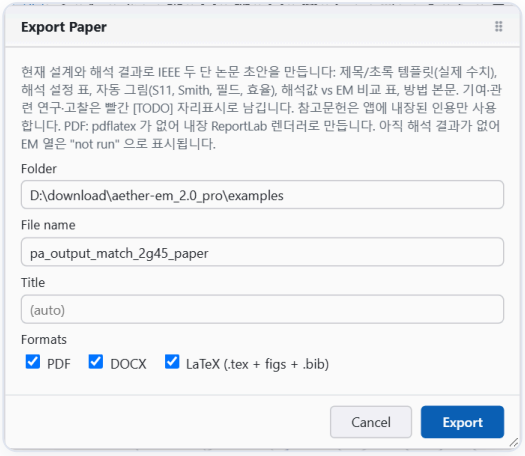


Figure 44-4 Export Paper. Folder, File name, Title (automatic if blank), Formats (PDF · DOCX · LaTeX). Without pdflatex, the built-in renderer makes the PDF.

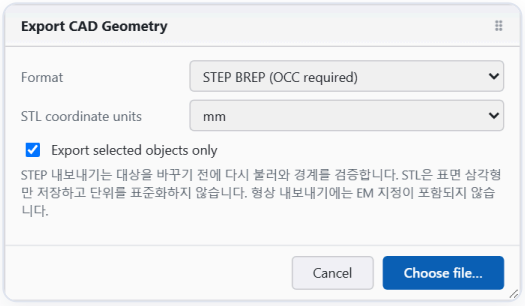


Figure 44-6 Export CAD Geometry. Format (STEP · BREP need OCC), STL coordinate units, Export selected objects only. Shape export does not include EM assignments.

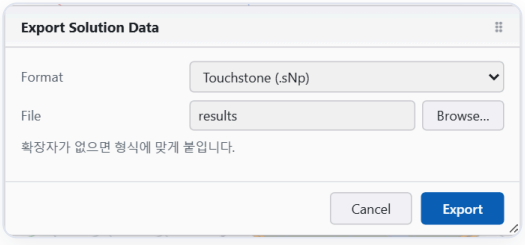


Figure 44-7 Export Solution Data. Format (Touchstone .sNp, etc.), File. If there's no extension, one matching the format is added.

45 CHAPTER

Reading Current · E · H · Radiation from One Dipole

We compare four kinds of results that come from the same solution, in one example. Seeing how the invisible phenomena interlock sums up the reading methods of Chapters 16–17 all at once.



You will learn
How S11 · Smith · Js · E · H · radiation connect

Try it
Solve examples/dipole_antenna.warp and rotate the phase

Key concepts
Where the current is large, H is large; at the ends, E is large

45.1 S11 and the Smith chart

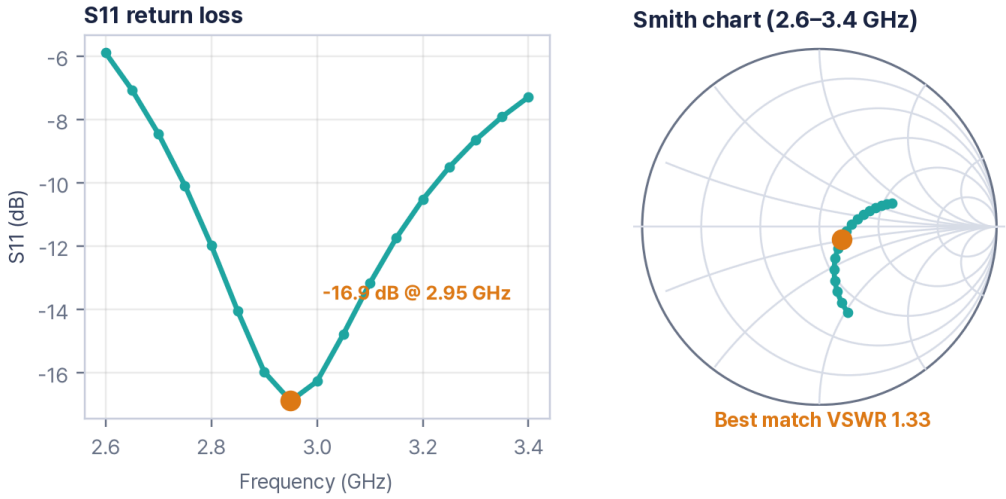


Figure 45-1 S11 of the dipole example (3 GHz class) (left), and the same points moved onto a Smith chart (right). It matches best at 2.95 GHz, at −16.9 dB and VSWR 1.33.

Best match	VSWR	Zin (at that point)
−16.9 dB @ 2.95 GHz	**1.33**	**64 − j9 Ω**

On the Smith chart, the closer the locus is to the exact center (50 Ω), the better the match. As frequency rises the locus turns clockwise, and the optimum is the point near the real axis. The upper half is inductive, the lower half capacitive.



A word from Aether
The lowest point of the S11 curve and the point near the center of the Smith chart **must be the same frequency**. If they're off, suspect the port reference impedance first.

45.2 Surface current `Results ▶ Surface Current |Js|`

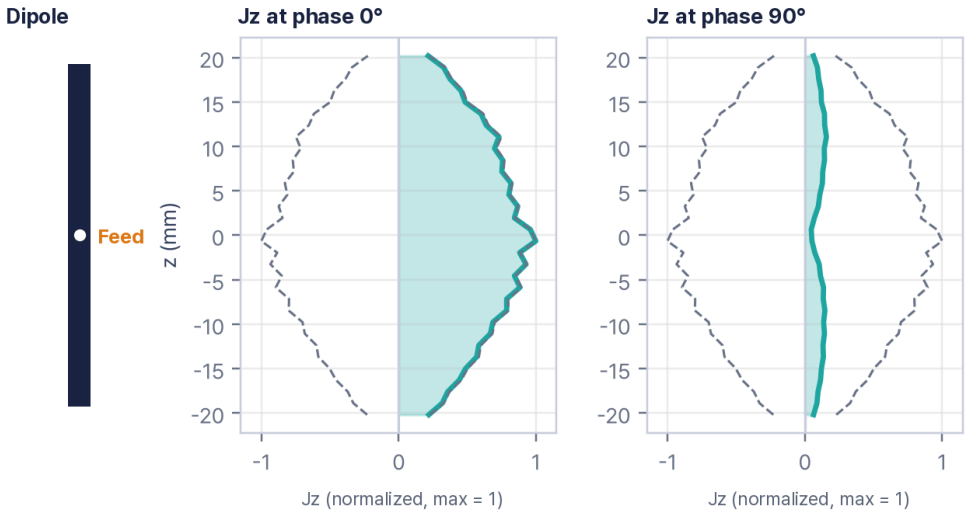


Figure 45-2 The z-directed current Jz on the dipole surface. The dashed line is the phase-independent magnitude (envelope), and the solid line is the instantaneous value at the specified phase. Values are normalized so the maximum is 1.

The current is a standing wave, **maximum at the feed point ($z \approx -0.7$ mm)** and decreasing toward the arm ends. At the arm ends the magnitude is about 23 % of the maximum. Rotate the phase by 90° and the instantaneous value drops to nearly 0, because the current and voltage are 90° out of step with each other.

45.3 E field and H field `Results ▶ E Field |E| · H Field |H|`

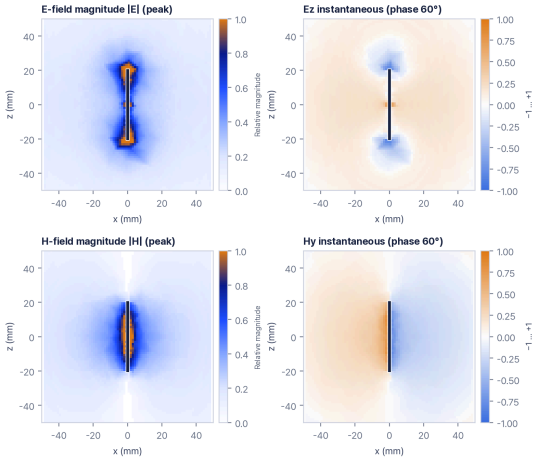


Figure 45-3 E (top) and H (bottom) on the x–z cut plane (y = 0). Left is the phase-independent magnitude, right is the instantaneous component at a phase of 60° (Ez, Hy). The color range is normalized so that the 99.5 % quantile, clipping the top 0.5 %, is 1.

- **E is strongest at the arm ends.** Excluding the feed gap, the maximum |Ez| is at the arm end (x = −0.6, z = −20.9 mm), because charge gathers at the ends.
- **H wraps around the current.** On this cut plane, Hy, normal to the plane, is about 98 % of the total field energy, and it is largest near the feed (x = 1.9, z = 4.4 mm).

45.4 Radiation pattern `Results ▶ 3D Radiation Pattern`

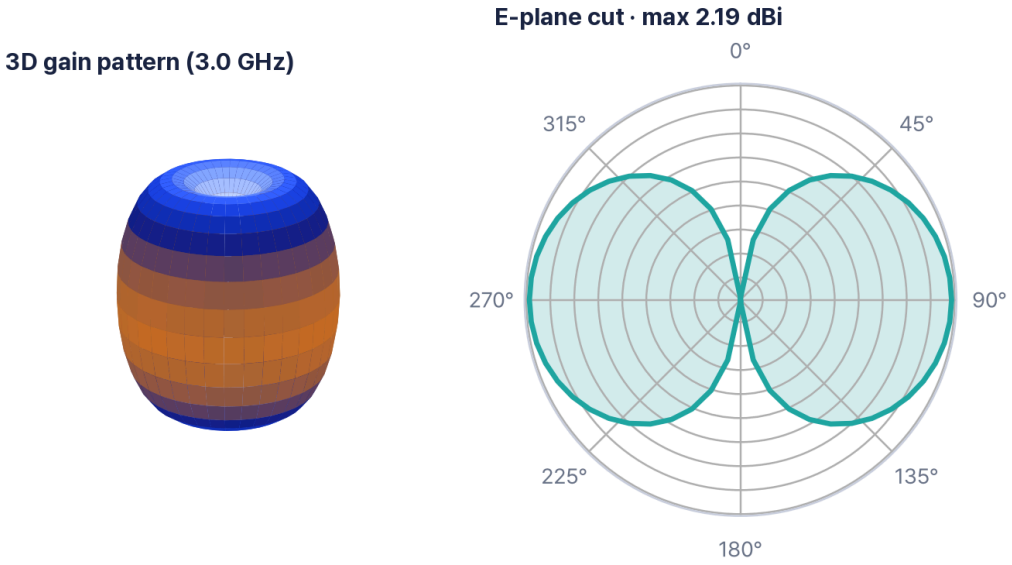


Figure 45-4 The 3 GHz 3D gain pattern (left) and E-plane cut (right). The radius is drawn proportional to the field amplitude, so the doughnut shape shows.

Max directivity	Theory (half-wave dipole)	Axial minimum
2.19 dBi	**2.15 dBi**	**−54.8 dBi**

A dipole radiates most strongly in the direction perpendicular to the arm axis (θ = 90°) and hardly at all along the axis. The variation with azimuth (φ) is about 0.05 dB — practically circular.

45.5 Linking the four results in one line

Result	What it tells you	What to suspect if it looks wrong
S11 · Smith	How much comes back from the input	Port reference impedance, resonant-frequency offset
Surface current Js	Which parts are used for radiation	A broken feed, unexpected current paths
E field	Where charge gathers (ends · corners)	Fake peaks where the mesh is coarse
H field	Loops around the current	If it should be symmetric but only one side is strong, an asymmetric feed
Radiation pattern	How much goes out in which direction	If a null tilts to one side, a boundary · ground problem



Wiz's warning

This example was solved with the default mesh (6,060 tetrahedra), so local values near the feed gap and corners may be rough. If you need exact numbers, reinforce the local mesh as in Chapter 17.

46 CHAPTER

Phase-2 Wireless Power: Tracking · Exposure · Pose · Rectifier · Resonator



Features added to the WPT Beam tab you learned in Chapter 26. Follow a moving receiver, keep within the limits when people come close, and calculate efficiency even when the pose changes.

You will learn
Moving-RX tracking, exposure map, RX pose, R_L, resonators

Try it
Run the figure-8 path in WPT Beam ▶ Tracking Demo...

Key concepts
Retrodirective re-aiming works without knowing the receiver's position

46.1 The menu at a glance NEW V2.3

Menu (WPT Beam)	What it does
Link Budget · Beamforming / Focusing · Distance Sweep	Link budget, steering vs focusing, power vs distance
Rectenna / RX · Field Slice / 3-D Beam · FEM Check	Receiver efficiency, field slices and 3D beam, FEM verification
Tracking Demo...	Re-aims at every step as the RX moves along a line · circle · figure-8 path
Exposure Map...	Beam-plane power density as a dB map relative to the limit, recommended transmit power
RX Position / Attitude...	RX position offset · tilt · rotation · polarization loss
Rectifier Load R_L...	PCE · Vdc vs load resistance
Resonator WPT · Cavity WPT · Cavity Resonator Designer...	Planar-resonator CMT link, automatic cavity-resonator WPT design

46.2 Following a moving receiver

As the RX moves along a path, it performs retrodirective re-aiming at every step (or every N steps). Noise of $1/\sqrt{(2\cdot \mathrm{SNR})}$ rad is added to the pilot phase, and the phase is quantized to the number of bits. It compares tracking, ideal tracking and a fixed beam.

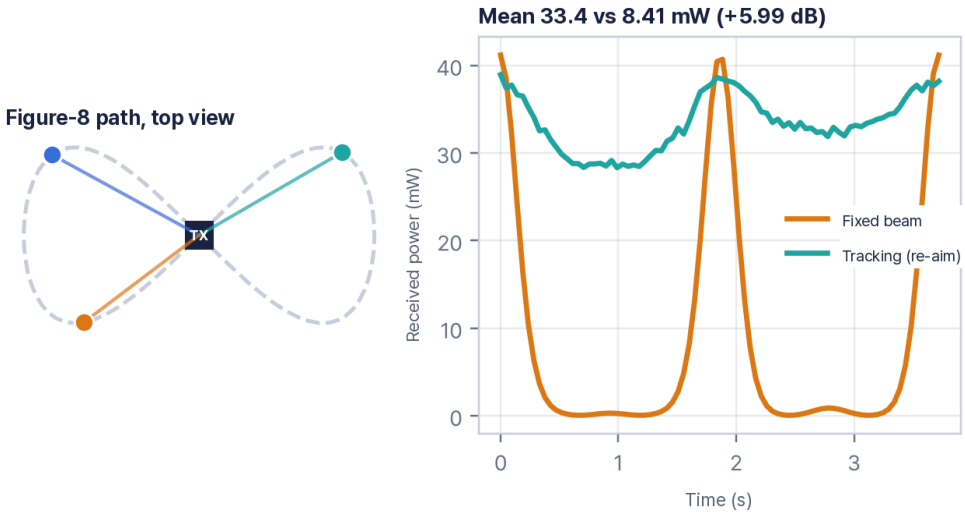


Figure 46-1 A figure-8 path (0.6 m, 0.5 m/s), 3-bit phase, pilot SNR 10 dB. Left: the path seen from above and the beam direction at three moments; right: received power over time. These are the values from running the tool's tracking calculation as-is.

Gain vs fixed beam	Mean received power	Mean DC	vs ideal tracking
+5.99 dB	**33.4 / 8.41 mW**	**21.4 / 5.2 mW**	**−0.35 dB**

The fixed beam drops to **0.03 mW** along the path, while tracking stays above **28.3 mW**. Even with 3-bit phase and an SNR of 10 dB, it is only 0.35 dB below ideal tracking.

46.3 Limits next to people `Exposure Map…`

Standard	Limit	Source
Korea general public 2–300 GHz	10 W/m²	Public Notice on Standards for Protection against Electromagnetic Fields No. 2019-4
FCC general public 1.5–100 GHz	1.0 mW/cm² (= 10 W/m², 30-min average)	47 CFR §1.1310 Table 1(B)
ICNIRP 2020 general public 2–300 GHz	10 W/m² (30-min average)	Health Phys. 118(5), Table 5
FCC occupational	5 mW/cm² (= 50 W/m², 6-min average)	47 CFR §1.1310 Table 1(A)

The white line on the map is the keep-out boundary where the density equals the limit. Assuming 'people don't come closer than r_min', it suggests the transmit power at which every point is below the limit, and **Apply suggested Pt** applies it directly. The example (8×8 array, 10 W, focused at 1 m) peaks at 1290 W/m², 129 times the limit, so for r_min 0.2 m a **21.1 dB back-off, about 77.8 mW**, is recommended. Enter the EIRP limit directly from the approval document.



Porty's check

The exposure map is a free-space point-source summation model. It ignores reflections and perturbation by the human body, so add measurement or FEM verification for final approval.

46.4 Even when the pose changes: RX Position / Attitude

The RX position is specified separately from the focus. Tilt (x · y axes) and rotation ψ are calculated from the element pattern and polarization projection (LP–LP, LP–CP 3 dB, CP–CP, dual-LP). Here are the losses for the example (offset 50 mm, tilt 30°, rotation 20°).

Mode	Offset	Pattern	Polarization	Total
focus (fixed)	0.58 dB	1.42 dB	0.42 dB	2.42 dB
retro (tracking)	0.03 dB	1.42 dB	0.42 dB	1.86 dB

The retro · optp · BCE display modes re-aim to follow the RX, so there is almost no offset loss. Mutual coupling and scan blindness of the RX array are not in the model.

46.5 Rectifier efficiency and load `Rectifier Load R_L…`

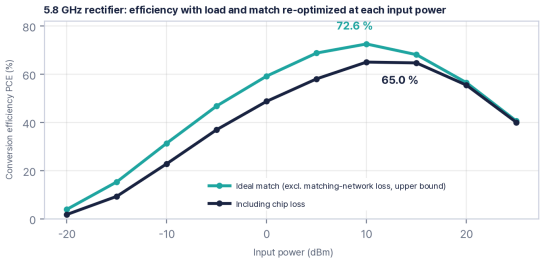


Figure 46-2 The conversion efficiency (PCE) of a 5.8 GHz rectifier. The load and match were re-optimized at each input power. 'Ideal match' is the upper bound excluding matching-network loss; including chip loss lowers the peak efficiency.

- Ideal-match peak **72.6 %** (10 dBm, input reflection −27 dB); peak including chip loss **65.0 %** (10 dBm).
- R_L sweep (10 dBm example): PCE 65.1 % at the optimum R_L ≈ 1159 Ω; at an input of 2000 Ω, PCE 45.2 % and Vdc 3.0 V (1.58 dB below the optimum).
- Efficiency drops sharply when the input power is low, and falls again when it is too high. For low-power designs, matching and diode selection are the key.

46.6 Cavity resonators and planar resonators

Tool	Contents (example)
Cavity WPT Designer	433 MHz, 500 W PA, robot area 0.4 × 0.4 m, height 0.25 m. TE101 cavity 496 × 250 × 483 mm, unloaded Q about 38,900, mean transmit efficiency about 94 % (design calculation)
Cavity Resonator Designer	Mode charts, Q, loop · iris coupling, miniaturization and PT-symmetric 2-cavity for rectangular · cylindrical cavities
Resonator WPT Designer	CMT distance links and PT-symmetric modes for spiral · SRR · meander · Hilbert · IDC-loop planar resonators, EM setup generation



A word from Wavy

The wavelength at 433 MHz is 0.69 m, so even a 2 × 2 array is 0.7 m across, and most of the inside of a cavity is the reactive near field. The free-space model only shows trends, so confirm real values with FEM that includes the cavity modes.

47 CHAPTER

AI Agents and Physical AI Integration

Aether has no built-in LLM. Instead, it is open so that AI agents such as Claude Code and Codex can work directly with the Python API, the CLI and text .warp files.



You will learn
Three entry points: CLI · Python · .warp

Try it
One turn of aether new → solve → validate

Key concepts
Files edited by an agent are checked with validate

47.1 How an agent runs the design loop

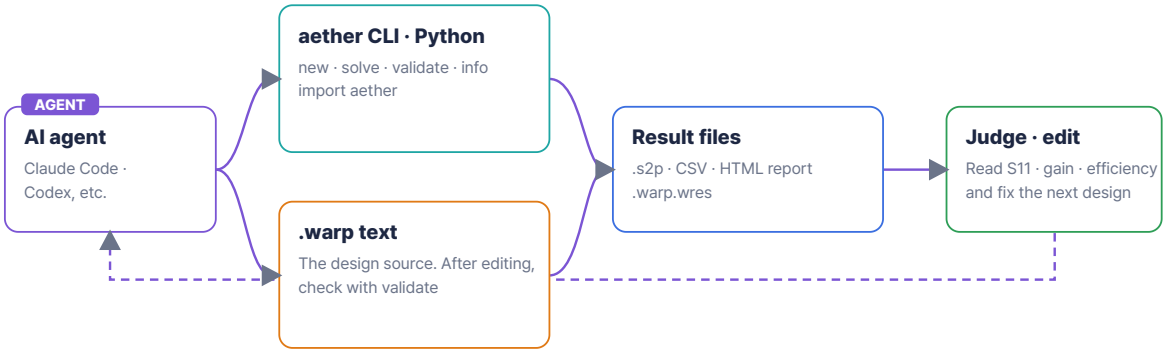


Figure 47-1 The loop in which an agent runs analyses through the CLI · Python, reads the result files and edits the .warp. The dashed line is the repetition of re-analyzing after an edit.

```
$ aether new demo.warp --template microstrip
  ports      : 2 → 2 excitation(s)
  setups     : Setup1
$ aether solve demo.warp --out demo_out
Solution for design 'PlateLine'  (10 frequency point(s), 7.37 s)
    pass 2:      212 tets,      1652 DOF, dS = 0.00003
    max singular value = 1.000000 (passive)
wrote demo_out.s2p, demo_out_sparams.csv, demo_out_modes.csv, demo_out_report.html
$ aether validate demo.warp
```

The output above is from an actual run. A .warp is human-readable text, so an agent can read and edit it. After editing, always check with `aether validate` and solve again.

47.2 Python API and prompt examples

```
import aether as ae
design, _ = ae.open_warps("examples/dipole_antenna.warp")
sol = design.solve(progress=False, save_fields=True)
print(f"{sol.sparams.db(1, 1).min():.1f} dB")                    # -16.9 dB
ff = sol.farfield(freq=3e9)
print(f"{ff.summary()['peakDirectivityDbi']:.2f} dBi")           # 2.19 dBi
```

Try asking an agent like this

- "Solve the examples/dipole_antenna.warp example and summarize the best-match frequency and maximum directivity in a table."
- "Create a microstrip project, analyze it, and tell me whether the S-parameters are passive."
- "Read this .warp, widen the line by 10 %, check it with aether validate, solve again and compare S11."

47.3 Physical AI: making power follow moving devices

Robots, drones and sensors move and change pose. To keep delivering power, the beam must follow their position, and that design is checked in simulation first. The tracking calculation of Chapter 46 is the core of this loop.

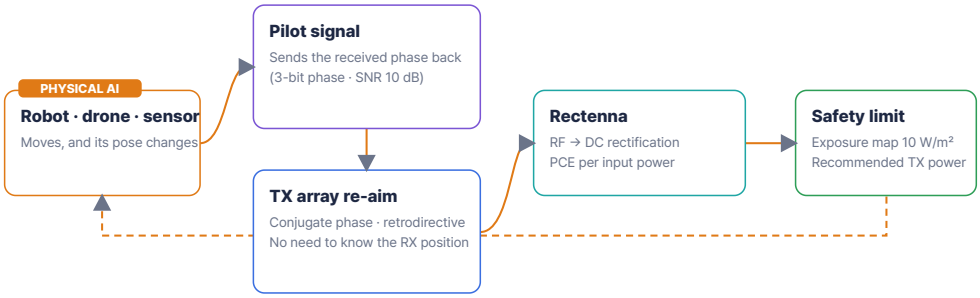


Figure 47-2 The closed loop of pilot → re-aim → rectify → safety limit. The agent explores the design space by changing this loop's parameters (phase bits, array size, transmit power).

- **Motion**: check the minimum reception along the whole path with moving-RX tracking (46.2).
- **Pose**: calculate tilt and polarization loss with RX Position / Attitude (46.4).
- **Safety**: keep within the limits next to people with the Exposure Map (46.3).
- **Exploration**: the agent reads the results of Parameter Study and Optimization (Nelder-Mead, Pattern, L-BFGS-B, Differential evolution) and fixes the next design.



A word from Wiz

Have the numbers an agent gives come from **the result files the tool calculated**. If you let the model state numbers from memory, they may be wrong.

48 CHAPTER

New Screen · Project · Data Features

The expanded screen display, file opening, multiple designs in one project, plot editor, parallel sweep and macromodel of Desktop 2026 V2.3, arranged in the order you use them.



You will learn
View styles · multiple designs · plot editing · macromodels

Try it
View the model 6 ways with View ▶ Look

Key concepts
Tell apart what changes only the display from what changes the analysis results

48.1 View styles (Look) and lighting NEW

`View ▶ Look` changes **only the display**. Selection · snapping · drawing · analysis stay the same, and the chosen style is remembered. You make the same choice with the palette button on the toolbar and ribbon `View ▶ Looks`.

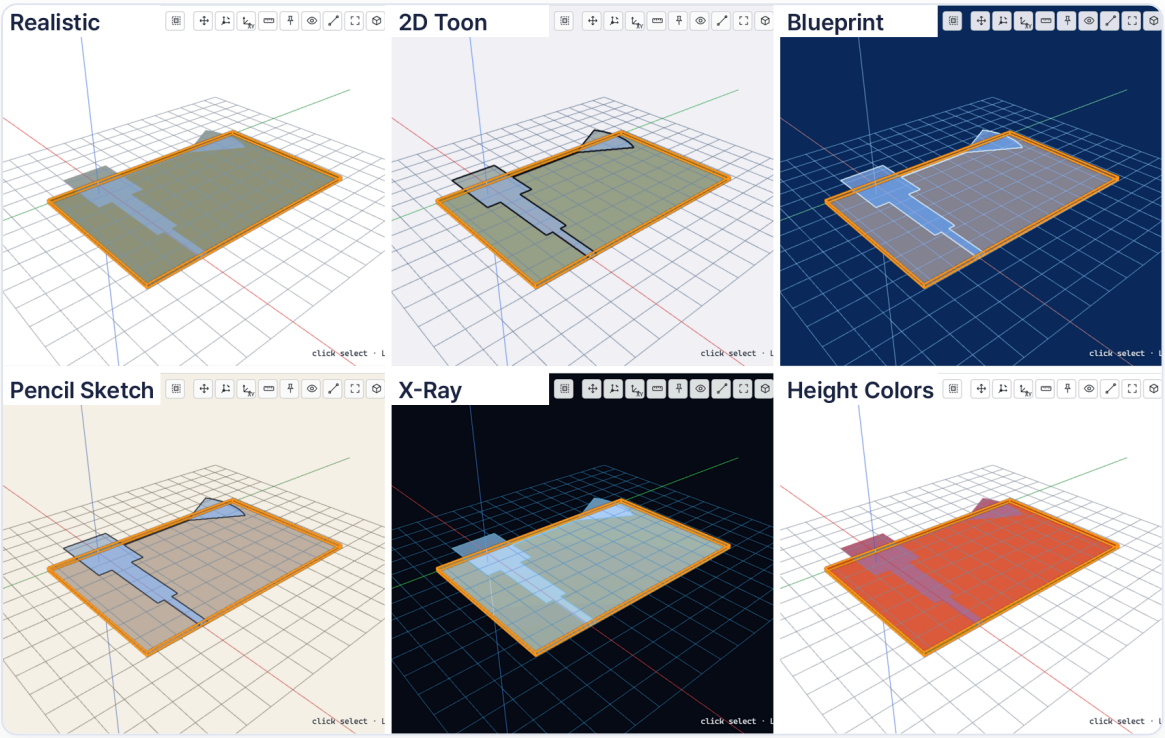


Figure 48-1 The same microstrip matching board seen in the 6 Looks (the selected substrate has an orange outline). From the top left: Realistic · 2D Toon · Blueprint · Pencil Sketch · X-Ray · Height Colors.

Style	Use it when
Realistic	Default. Realistic display with material colors and shading.
2D Toon (webtoon)	Flat-color faces, ink-line outlines. Clean for presentation slides and document figures.
Blueprint	Blueprint style. For explaining structure.
Pencil Sketch	A sketch style where shadows are drawn as hatching.
X-Ray	See-through like glass, so every layer · via · sheet shows at once. Good for checking internal structure.
Height Colors	Shows each body's z height as color, with a legend. For checking the layer stack-up.

Lighting (View ▶ Lighting) lets you choose Camera Headlight (default, follows the camera) · Work Plane · Fixed (the old way); Brighter / Dimmer adjust by 10 %, Brightness... sets it directly, and Reset restores it.

`View ▶ Auto Display on Open`, when on, hides regions · PML and shows conductors opaque when opening a file (off keeps the saved state). Show hidden regions again with `Show Regions / PML`.



Wavy's tip

Click the **small disc** under the axis triad and you get the view from that direction (top → from above, bottom → from below). Wheel zoom is centered on **the point under the cursor**.

48.2 Opening files and new-project templates NEW

- **Column widths**: drag the dividers in the Name · Size · Modified headers to change width; double-click to fit the longest entry. Remembered.
- **Type to find**: type a letter in the list to jump to a name starting with it. Press the same letter again for the next entry; for Korean names, typing just the initial consonant (ㄱ) works.
- **.warp preview**: a 3D view to the right of the list (drag = rotate, right · Shift drag = pan, wheel = zoom, double-click = fit) plus name · object count · size · modified date. It doesn't read the CAD source, and shows only the saved size as a box.
- **Recent files**: 5 appear above Exit in the File menu and as cards on the empty workspace.

`File ▶ New from Template…` has 18 templates by purpose, in four branches — basics, antennas, RF circuits and PCB, analysis tools — and each template comes with a description and the order in which to try out its features. Templates open as **unsaved copies**, so no temporary files are left in the recent files.

48.3 Multiple designs in one project NEW

As in HFSS, you can keep several designs inside one .warp. Each design has its own shapes · boundaries · ports · analysis settings · results · co-simulation settings · undo history **separately**.

HOW TO **Adding and switching designs**

1. Add an empty design with `Project ▶ Insert ▶ Warps Design` (existing designs stay). For eigenmode, Warps Eigenmode Design.
2. To bring in a design from another file, `Insert Design from File…`. If names clash, a number is added, as in WarpsDesign3.
3. Click (or double-click) a design in the project tree to change the active design; any open windows close.
4. Right-click a design for Set as Active · Rename · Duplicate · Delete. Duplicate copies shapes · settings · reports, but not solutions.
5. A single **Save** stores all designs in one .warp, and the last active design is remembered.

- `File ▶ Open Project…` replaces the whole project (different from adding a design).
- The last remaining design can't be deleted. Use Close Project.
- The project tree is **grouped by material**, and the group color applies to all objects of that material. Ctrl · Shift select multiple items.

48.4 Measurement and info tables NEW

The measurement window (`Edit ▶ Measure / Dimensions…`, shortcut M), `Tools ▶ Engineering Diagnostics…`, `Results ▶ S-Parameter Metrics…`, `Edit ▶ Warps Import Status…` and via · bondwire readouts now come out **as tables**: headline values at the top, Item | Value rows below, and an X / Y / Z grid. Turn on **Keep on screen** and the values stay where you measured (a dimension line with arrows) and move with the camera.

The snap radius is fixed at **10 px on screen**, and it snaps not only to edges · endpoints but also to **circle and arc centers · quadrant points**. `Edit ▶ Move by Two Points…` (Ctrl+M) doesn't change Z while moving.

48.5 Plot editor: into report-ready figures NEW

All x–y graphs of results (S-parameters, antenna gain · efficiency, far-field cuts, formula graphs, fields on a line, convergence, comparison, co-simulation · rectifier figures) are drawn in **report-figure style**: white background, black frame with outward ticks, light grid, axis names with units, a true minus sign, lines + markers, a legend placed in the emptiest corner, a right Y2 axis, dashed target lines and vertical markers.

HOW TO **Polishing a graph**

1. Press ✎ **Edit plot** on the graph toolbar, or double-click the title · axis area.
2. In the **Axes** tab, change the title, X · Y · Y2 names, range (auto / fixed), log axis, grid, legend position and font size.
3. In the **Traces** tab, set each curve's visibility · name · color · line style · width · marker · move to Y2.
4. In the **Lines & notes** tab, add target lines (e.g. −10 dB), vertical lines and notes with arrows. The m1, m2 markers can be turned into notes or lines.
5. In the **Export** tab, get PNG (2× resolution), SVG or CSV. A style you adjust once also applies to the next result of the same kind (**Reset style** to reset), and is not saved in the .warp.

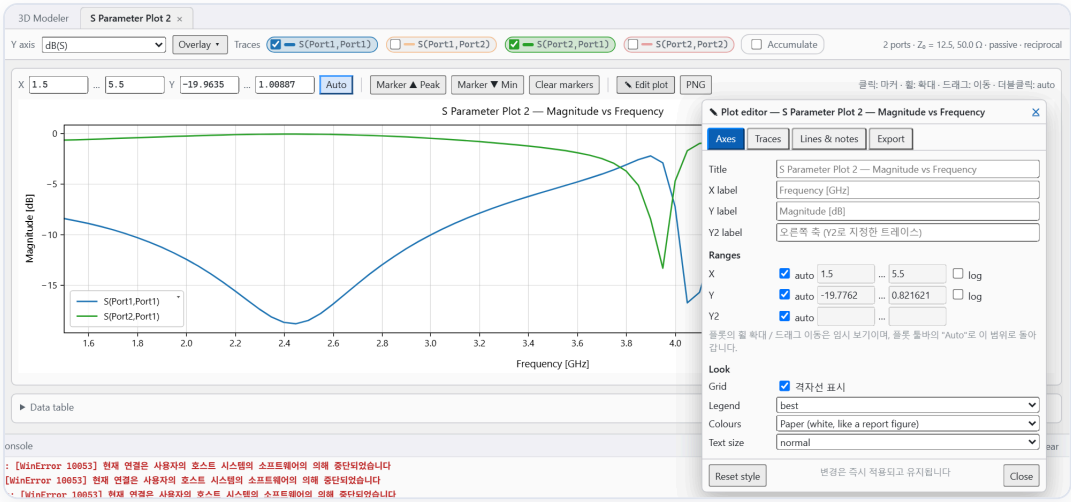


Figure 48-2 An S-parameter graph and the Plot editor (right). The Axes tab has title · axis names · range (auto / fixed) · log · grid · legend position · color scheme (Paper) · font size, and Reset style at the bottom restores them. Changes apply immediately and persist.

The editor is a floating panel, so it doesn't close when you click outside it, and you can keep using the 3D view. Drag the title bar to move it, and close it with Esc · × · Close.

48.6 Parallel frequency sweeps UPGRADE

All frequency solves of a Discrete sweep, and the seed · probe · verification solves of an Interpolating sweep, are split across several worker processes. The setting is at `Edit Setup… ▶ Solver acceleration ▶ Sweep workers`, and the environment variable is `AETHER_SWEEP_WORKERS`.

Value	Meaning
0 (default)	Automatic. One worker per 3 threads, limited by the remaining memory. Not used for sweeps whose work is under about 12 seconds.
1	Off (sequential)
N	N workers

Answers match the sequential run to about 1e-13. If workers can't start or one dies, the remaining points are solved in the same process. On a 12-core PC, a 163k-unknown model gained 1.15× (3–6 workers) to 1.3–1.5× (8 workers × 3 threads); memory bandwidth is the limit, so the improvement on a single machine is not large.

48.7 S-parameters into a SPICE macromodel NEW

`Results ▶ Vector Fit / SPICE Macromodel…` fits the analyzed S matrix with rational functions and lets you download a **.subckt** (for SPICE · Xyce · Qucs-S). The dialog shows the order, rms · max error, whether it is passive and where violations are, and you can try enforcing passivity (best effort; it may not converge, and the result says so). At least 8 frequency points are needed, and the reference impedance is real for SPICE ports (default 50 Ω).

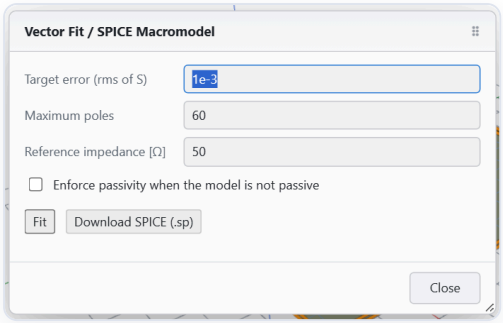


Figure 48-3 Vector Fit / SPICE Macromodel. Target error (rms of S), maximum poles, reference impedance, enforce passivity, Fit, Download SPICE (.sp).

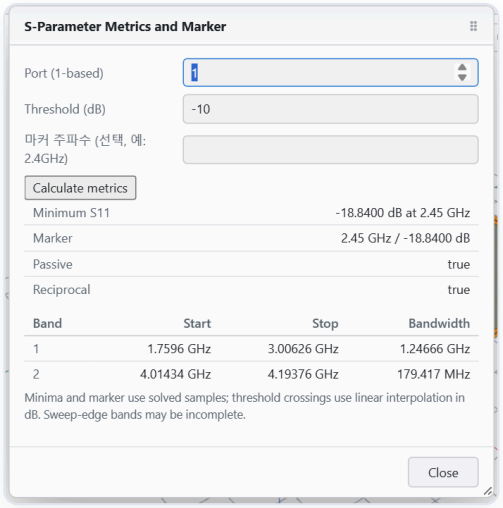


Figure 48-4 S-Parameter Metrics and Marker. Enter the port and threshold (dB) and press Calculate metrics, and the minimum S11, marker value, passivity · reciprocity and each band's start · stop · width come out as a table.

```
# Optional packages you need
pip install scikit-rf      # Vector Fit / SPICE Macromodel  (extra: rf)
pip install optuna         # Optimization ▶ Method ▶ Bayesian / TPE  (extra: opt)
```

Bayesian / TPE optimization is chosen under Method in `Tools ▶ Optimization…`. Use it when each solve is expensive and you want to minimize the number of solves; it starts from the current design. The other methods are Nelder-Mead · Pattern · L-BFGS-B · Differential evolution. Before opening optimization, you must define **design variables** and **link them to the primitive dimensions** (otherwise the status bar shows a hint).

48.8 Arbitrary-direction cut plane in the exported 3D viewer UPGRADE

Besides the X · Y · Z cut planes, the viewer made in Chapter 44 has **one cut plane defined by a normal and a position d** (slider or number). Set the normal by typing into the three boxes, or with the X / Y / Z, **View** (viewing direction) and **Flip** buttons. **Probe** moves it to pass through the clicked point. It samples the saved volume grid, so the file size doesn't grow (only about 13 KB of code is added), and Export's **Volume grid** must not be Off. It has been fixed so the moving cut plane isn't dropped entirely even when the target size is exceeded.

48.9 Where terms and defaults changed IMPORTANT

Item	Before → now
Basis-order names	The former 'First order' (6 unknowns per element) → **Zero order**, the former 'Second order' (20) → **First order**, plus **Mixed**. Saved values (1, 2, 3) are unchanged, so projects open with the same order.
Order in new analysis setups	**First order** is the default (saved setups are unchanged)
BasisOrder in Warps files	Read as Warps numbers: −1 Mixed, 0 Zero order, 1 First order, 2 is First order (with a note)

Convergence criterion	Convergence over 2 or more consecutive passes is the default; Zero order needs at least 3 passes · 2 convergences, and warns if the mesh grows less than 1.5× and converges
Sparse discrete sweep	If the spacing exceeds 5 % of the band, Validate · the message window · the solver log warn and recommend a Fast / Interpolating sweep or a spacing of about 2.5 % of the band.
Mixed order	Fixed to concentrate first order on high-energy elements; faster than First order.
Eigenmode solve	Same convergence rules, and solved with PARDISO for lower memory (below 20k unknowns, the old method as before).

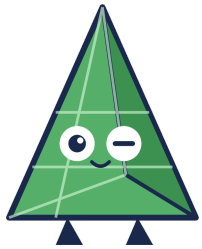


Wiz's warning

The 'first order · second order' that appear in Chapter 14 and elsewhere in the main text are **the old names**. The names on screen are Zero order · First order, so read the book's first order = Zero order on screen, and the book's second order = First order on screen.

49 CHAPTER

New Modeling Features: Bondwire · Chip Parts · Vias · Stubs · SMD



The tools you reach for when drawing RF boards have moved closer to real parts and manufacturing rules. Here is the order to use them and what to watch for. Step-by-step lab examples are in Chapter 9 (bondwire · Via Fill · chip parts · meander · stubs).

You will learn
Bondwire, real chip parts .s2p, Via Fill, L/C stubs

Try it
Put a Murata 0402 capacitor into a Lumped RLC

Key concepts
The difference between ideal elements and real parts

49.1 Bondwire `Draw ▶ Bondwire…` NEW

Like HFSS's Bondwire, draws a wire from **a pad point → a lead point**. Enter the points directly or click them in the view with Pick (snapping applies), and swap the two points with the ↔ (Swap) button. The wire is **a real solid** (a regular N-gon cross-section, a sweep with mitered joints), so it is analyzed as-is.

Shape	Path (pad at origin, lead at (D, −h2))
JEDEC4	(0,0) → (0,h1) → (D/8,h1) → (D,−h2)
JEDEC5	(0,0) → (x1,h1) → (x1+D/8,h1) → (D/2, −h2+(D/2)·tanβ) → (D,−h2), x1 = h1/tanα
Low	(0,0) → (x1,h1) → (x2,h1) → (D,−h2), x2 = D − (h1+h2)/tanβ

- **Embed ends**: buries both ends d/2 into the pad · lead so the faces don't misalign during assembly and the wire merges with the pad into one.
- Impossible values (combinations of h1, α, β) are corrected with a warning. Wire walls are meshed at twice the diameter and treated as thin round lines.
- **.warp storage**: stored as HFSS's BondwireParameters (WireType, WireDiameter, NumSides, Pad pos, Dir, Distance, h1, h2, alpha, beta, WhichAxis), so bondwires from HFSS projects are also read as solids. Count · pitch · end embedding are Aether-only keys.

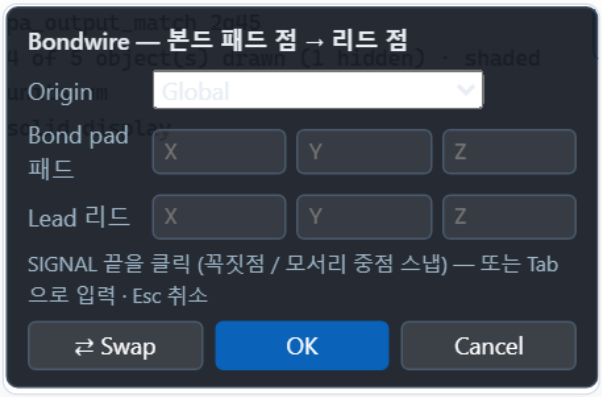


Figure 49-1 The Draw ▶ Bondwire... input window. Fill it by entering the Origin, Bond pad and Lead coordinates, or by clicking points in the view.

49.2 Real chip parts .s2p `Lumped RLC ▶ Real part` NEW

For lumped RLC boundaries and SMD parts, choose the model from **Ideal | Real part (.s2p) | Fitted circuit**. Real part uses as FEM coefficients an impedance table Z(f) converted from the manufacturer's S-parameters to suit the series · parallel connection; Fitted circuit is a model fitted to it as an equivalent circuit.

- **Library location**: `libraries/murata` under the project folder. Change it with the environment variable `AETHER_CHIP_LIBRARY_DIR`. The Library folder path is shown at the top of the window, with Copy path and **Rescan** buttons.
- **Bundled parts**: the 54 0402 files published by Murata (MLCC GJM · GRM, inductors LQW15AN-00 · LQG15HN-02, 25 °C, 0 V bias), unmodified.
- **Automatic scan**: opening the library reads the .s2p files in the folder and subfolders, re-reading only changed files. Part number · type · value · size are read from the Murata file names.
- **Import directly**: Import .s2p... (several at once), Import folder... (including subfolders), or Browse to an .s2p file directly in the model field.
- **Portability**: the part data goes inside the .warp, so the same results come out on another PC. Older projects open as Ideal.



Porty's check

An ideal 0.5 pF capacitor and a real 0402 part can differ quite a bit in impedance at 5.8 GHz because of self-resonance and ESR. For circuits with sensitive matching, always check with **Real part**. The files are 25 °C · 0 V data, so temperature and bias changes aren't reflected.

49.3 Via Fill / Smart Via `Modeler ▶ RF ▶ Via Fill / Smart Via…` NEW

Fills a selected copper face (any outline) with vias. Use it to make a ground via fence or a thermal via array in one go. If you select an object that isn't a copper area (e.g. the substrate), it tells you 'select the copper area to fill'.

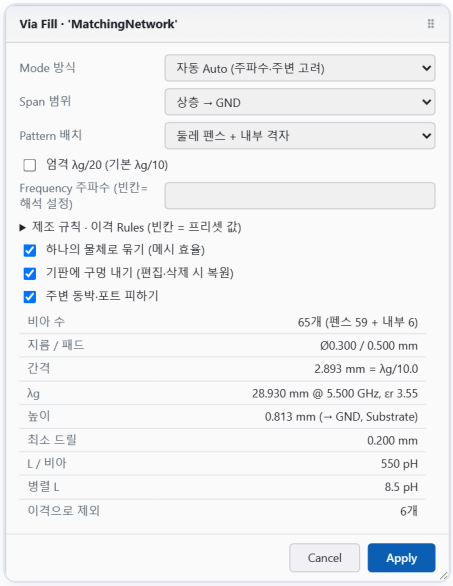


Figure 49-2 The Via Fill dialog (e.g. 65 vias on a microstrip matching network). Mode is automatic (considering frequency and surroundings), Span is top layer → GND, Pattern is perimeter fence + inner grid (spacing in this example 2.893 mm = λg/10), and below it calculated results such as via count · diameter/pad · spacing · height · minimum drill are shown.

- **Mode**: automatic (Auto, considering frequency · surroundings) and manual rules. The spacing defaults to λg/10; turning on the 'strict' option makes it λg/20.
- **Manufacturing rules · clearance Rules**: leave blank to use the preset values.
- **Options**: merge into one body (mesh efficiency), cut holes in the substrate (restored on edit · delete), avoid surrounding copper · ports.
- The vias created are managed with the rules · list · edit · delete · sync commands.

49.4 Making C · L from a line `Modeler ▶ RF ▶ C / L from a Line…` UPGRADE

A tool that attaches a stub beside a line to make the C or L you need. You can now **choose the stub shape**.

Shape	Characteristics
Rectangle	The same rectangle as before. An open stub is −jZ0·cot β(l+Δl) (Hammerstad's Δl).
Round pad	A round pad
Radial (fan)	A fan. Default angle 60°, editable.
Regular N-gon	A regular N-gon (with a flat side toward the line)

- Every shape is solved by **its input impedance at the connection point**, and the result shows the value the model returned (quasi-static · lossless model).
- The connection point is always the feed-side end of the line, and circles · polygons connect with a strip the width of the line. A **3D preview** appears in the view.
- Placement is **one side** (the drawn side + or the opposite side −) or **both sides** (two mirror-symmetric stubs at the same point, e.g. a fan pair).

49.5 SMD parts and SMD @ Point UPGRADE

- **Angle**: in the SMD Part dialog, set the pad1 → pad2 axis to any in-plane angle (on the XY plane, 0° = +X, 90° = +Y, automatic if blank). SMD @ Point has 0 / 90 / 180 / 270 quick buttons and free angle input.
- **Preview**: turn on `Place SMD at Point…` and hover over a point, and the part appears as a semi-transparent 3D ghost (real size and Z) with the target body highlighted. Click to lock it, Enter to place, Esc to unlock · cancel, Re-pick to choose again.
- **R / Shift+R**: rotates the selected objects ±90° about the Z axis (about the center of their common bounding box, undoable, ignored while typing text).

49.6 Meander `Modeler ▶ Meander…` UPGRADE

With **Fix length** on (default), the line length is fixed and the number of turns · height · width are redistributed. Turn it off and the length field is released, so the line can grow or shrink. The dialog has a **live preview** and a readout of turns · height · width · length (e.g. `length 24mm (+4mm)`), and impossible combinations are explained with a red reason (e.g. 9 turns won't fit). The length is also shown while dragging an end.

49.7 Open Region and other cleanups

- **Create Open Region** (Simulation menu): set the frequency and absorption method, and an air box and boundaries sized to the wavelength are created. **Radiation** is λ/4 from the model, with a first-order radiation condition on all open faces. **PML** is an air gap of λ/8, PML thickness λ/4, then PEC, with a graded design for 1e-3 reflection. Open faces can be changed individually (keep ground planes or walls closed), and the dialog shows the box size in mm and wavelengths. Eigenmode designs don't accept PML.
- **Smart Connect / Auto Feed**: reads the endpoint layer from flat copper, Edit (Re-run) has a **Replace junctions** option, and conversions persist when re-run. Apply, which used to hang on large feed networks, is fixed, and display building has a time limit (default 90 seconds).
- **KiCad / Gerber copper** can also use **RF ▶ Step to RF Line**, like STEP, to cut straight lines and use Meander · Stub · Z0 Line, etc.
- **Surface current on finite-conductivity sheets** was fixed to reflect the elements on both sides (previously it showed only the air side, sometimes displaying only about 10 %).
- **Modeless dialogs**: you can rotate and pan the 3D view while a feature window is open, and they don't close on an outside click. Enter during Korean input and number + unit fields are also stabilized.

50 CHAPTER

New PA · Rectifier · Thermal · Antenna-Wizard Features



Features added on the amplifier · rectifier · cooling · antenna-wizard side. The biggest change is that changing a number in the PA Tuner recalculates the whole amplifier in 0.1 seconds. See also Chapters 23–25 (PA · rectifier), Chapter 24 (PA Tuner) and Chapters 27–30 (thermal analysis) for cases and figures.

You will learn
PA Tuner · PA Results · rectifier report · antenna auto-tuning

Try it
Results ▶ PA Results ▶ PA Tuner (live, editable)

Key concepts
Tune fast, finalize with EM

50.1 PA Tuner: change it and it recalculates right away NEW

`Results ▶ PA Results ▶ PA Tuner (live, editable)` turns the window that only displayed the results saved by PA Wizard into **an editable calculator**. Each time you change a number, it recalculates the whole amplifier in about 0.1 seconds from the information stored in the design (EM network, chip, port roles).

Block	Contents
① **Behavioral PA model**	Class, Psat, DE, Vdd, Idq, compression, gain expansion, AM-PM
② **Output load model**	Maximum-power load and contour sharpness (0 = off). The Psat loss follows the load the board presents to the drain.
③ **Matching trimmers**	Attaches shunt C · L, series L · C and lines at the 4 EM ports, connected exactly to the N-port S matrix
④ **Thermal · cooling**	In the power sweep, Pdc + Pin (accepted power) − Pout; junction temperature and Tj-limit margin for every cooling design in the project, maximum Pout under the limit, optional gain · Psat temperature coefficients

- **Auto-tune**: finds the checked trimmers for the targets (worst S11, gain level · ripple, Psat loss, μ) with differential evolution + Nelder-Mead, penalizes large changes, and snaps to E24 or 0.1 pF / 0.1 nH values.
- **Yield**: runs Monte Carlo over part tolerances.
- Checking items doesn't rebuild the panel, so open sections · collapsed states · scroll position are kept.
- **Cooling designs are characterized only once.** For each design with a device, it runs thermal FEM at 0.5 · 1 · 1.5× power and stores the R_ca(P) curve and thermal-path segments (a bare package is 15–27 % nonlinear, so a single resistance is wrong). Projects that have thermal designs but no characterization do it automatically the first time the tuner opens.



Porty's check
The temperature-dependent gain · Psat correction is an electro-thermal fixed point with **efficiency held fixed**, so it is optimistic. Do the final check with thermal FEM.

50.2 New groups in PA Results `PCB analysis · Thermal`

PA Results under the Results menu has the groups Summary · Power sweep · Efficiency · Frequency · Linearity · Load and layout · Simulation · **PCB analysis** · **Thermal**.

- **PCB analysis**: return loss of the 4 EM ports, dissipation of the two matching networks (−10 log MAG, independent of termination; S21 into 50 Ω in an impedance-transforming network is not loss), amplifier S11 · S22 · gain with target lines, Psat, Smith chart.
- **Thermal**: heat and junction temperature vs input power, Pout under the Tj limit, Tj vs ambient temperature, operating point vs cooling, thermal path.
- A **load model** (zoptOhm, loadK; loadK = 0 turns it off) can be entered directly in the PA co-simulation, so even library chips without a datasheet load have a Psat that depends on the matching.

50.3 Rectifier report and co-simulation NEW

- **Results ▶ Rectifier Report... / Rectifier Plots...**: creates a Pin sweep, power budget, BV (breakdown voltage) warning and CSV all at once from the Nonlinear Co-sim setup. The plots are efficiency vs input power · load R_L · frequency f0.
- **Tools ▶ Nonlinear Co-sim** has numbered steps (① network ② port roles ③ sweep ④ run ⑤ results), hints for each step, and a pre-run checklist (network loaded, exactly 1 Source, Diode, DC load, data up to K·f0).
- **R_L · f0 sweeps**: re-solves harmonic balance per load resistance or frequency to draw efficiency curves.
- **Setup restoration**: after saving and reopening, port mapping · Touchstone (embedded in the .warp) · diode · chip parts · DC load · sweeps are restored. Touchstone export writes `! Port[i] = NAME` comments.
- HB convergence of voltage-doubler · series-diode rectifiers is improved, so 12 dBm-class inputs also solve.
- **Tools ▶ Device Library...**: only diode models with a cited datasheet source are built in (HSMS-282x / 285x / 286x, SMS7630 / 7621 / 1546 / 3922 – 3924, NT9000 – 9003). BAT15 · BAT62 have no public SPICE models and must be imported yourself.

50.4 PA chip library and PA Wizard NEW

- **Tools ▶ PA Library...**: 17 chips · modules from 9 manufacturers (NXP, Ampleon, MACOM, Mini-Circuits, etc.). The same library is used for PA Wizard's operating point and the PA block of Nonlinear Co-sim.
- **Applying a chip**: PA Wizard gets Vdd · Idq · class · Psat · efficiency · datasheet Zs/Zl filled in, and in co-simulation it is connected between the corresponding EM-network ports in the PA input (gate) / PA output (drain) roles.
- **Reading circuits**: reads KiCad .kicad_sch (restoring nets from wires · junctions · labels · power symbols · rotation · mirrored pin positions) and KiCad · ADS · Qucs netlists. Parts without a device form aren't silently dropped but listed as 'unmapped'.
- **Performance output**: Analyze & Design opens a **PA performance** tab for the selected candidate pair, showing Pout · gain · DE · PAE vs Pin, P1dB · Psat, AM-AM / AM-PM and back-off efficiency.
- **Simulation tab**: Draw into design → Solve (EM, a few minutes) → Simulate combines the device S2P with cable · ferrite models and shows the RF_In → RF_Out S-parameters and stability next to the circuit estimate.
- **Low-frequency layout**: drain · gate bias longer than 60 mm is built with a chip RF choke + bypass capacitor and vias instead of a printed λ/4 (50–512 MHz demo board, 80 × 27 mm).
- Every wizard window has a **How to use** banner and one-click examples (antenna 8, PA 4, transmission line 5, matching 5), input-check messages, a calibration badge per candidate, and a **Next steps** panel after Create design.

50.5 Antenna wizard: it now draws all 22 families UPGRADE

Previously only patch arrays · FPRA · AMC dipole · quasi-Yagi · PIFA could be drawn; now **all 22 families** can create designs.

Family	Notes
Circular · stacked · E-shaped patch, series-fed comb-line	Probe-fed patch arrays include a corporate feed network under the ground (λ/4 transformer T-splits) in the design.
AMC dipole, printed LPDA, Vivaldi, axial-mode helix, Archimedean spiral, crossed dipole	Crossed dipoles use ports at 0° / −90°; families without a planar feed are automatically excited in phase with Edit Sources.
SIW horn · SIW slot array, cavity-backed slot, dielectric resonator, meander monopole	SIW uses continuous PEC side walls; cavities are PEC boxes.
Reflectarray panel, 2-layer FPRA	Reflectarrays have no feed · ports and are for layout and export.

- **EM auto-tuning (Overview tab)**: draw → solve → find the S11 minimum and Re(Zin) peak → scale the radiator length (k_len) proportionally and move the feed (target resistance = 50 + $X^2/50$), and repeat. The best pass is kept, and Create design draws the tuned antenna. It runs in the background and can be stopped with **Stop**.
- **Calibration evidence**: each candidate gets a calibration badge, and its description honestly states on which substrate it was matched against Aether FEM (e.g. circular patch on RO4350B 0.508 / 1.524 mm, at 5.8 GHz after tuning 5.805 / 5.796 GHz, S11 −15.9 / −28.9 dB).



A word from Aether
The wizard is **'the starting line'**. After drawing, solve it with EM, and polish it with auto-tuning or the PA Tuner if needed. Substrates · frequencies outside the calibration range of the synthesis formulas may have larger errors.

50.6 Thermal workbench summary UPGRADE

There is an independent **Thermal** tab. In addition to the content of Chapters 27–30, remember the following.

- **Tree**: Setup · Materials · Sources · Boundaries · Interfaces · Results. Every field has a Korean tooltip, and help is in `Thermal ▶ Thermal Guide`.
- **Heat sources**: transistor (Pout / η / gain → Pdiss, Rth j-c → Tj and margin), RF loss → heat (dielectric loss $½\omega\varepsilon_0\varepsilon''|E|^2$ and wall loss $½R_s|H_t|^2$ from the solved fields, excluding reflection · radiation).
- **Boundaries · interfaces**: per-face convection, radiation (Newton), fixed temperature + contact resistance, adiabatic, contact resistance / TIM presets, thin copper shell (oz × layers).
- **Helpers**: Via Wizard (equivalent anisotropic k), Copper Coin, Heat Spreader, PCM (enthalpy), Pulse / Duty, Temp → RF feedback, Optimize Tj, Heat Path graph, Export Field CSV. Examples Th1–Th8 are included.
- Even with thermal settings, **the S-parameters don't change** (maximum $|\Delta S| = 0$ in example verification).

10.X Field cheat sheet: the new features on one page

What you want to do	Menu · command	Ch.
Check settings before analysis	Simulation ▶ Setup Advisor... → Apply selected	43
Send 3D results to a colleague	File ▶ Export 3D Viewer (three.js)... (turn on Save fields)	44
S-parameters to another tool	Results ▶ Export S-parameters... (.sNp) · CSV	44
Paper draft · PDF report	File ▶ Export ▶ Paper... · Export Report...	44
View current · fields · radiation	Results ▶ Surface Current · E Field · H Field · 3D Radiation Pattern	45
Track a moving receiver	WPT Beam ▶ Tracking Demo...	46
Safety limits next to people	WPT Beam ▶ Exposure Map... → Apply suggested Pt	46
Pose and polarization loss	WPT Beam ▶ RX Position / Attitude...	46
Optimize the rectifier load	WPT Beam ▶ Rectifier Load R_L...	46
Cavity WPT for a robot area	WPT Beam ▶ Cavity WPT Designer...	46
Automate with an AI agent	aether new · solve · validate · info / import aether	47
View the model in another style	View ▶ Look ▶ 2D Toon · Blueprint · X-Ray ...	48
Add a design to a project	Project ▶ Insert ▶ Warps Design	48
Turn a graph into a report figure	Graph ✎ Edit plot → Export PNG / SVG / CSV	48
S-parameters into SPICE	Results ▶ Vector Fit / SPICE Macromodel...	48
Bondwire · via fill	Draw ▶ Bondwire... · Modeler ▶ RF ▶ Via Fill / Smart Via...	49
Use real chip parts	Lumped RLC / SMD model ▶ Real part (.s2p)	49
Tune by changing PA numbers	Results ▶ PA Results ▶ PA Tuner (live, editable)	50
Rectifier efficiency curves	Results ▶ Rectifier Report... / Plots...	50
Find every menu on screen	PART 11 Menu · ribbon reference	11
The screen looks odd after an update	Browser Ctrl+F5	43



Aether's closing word

If you've come this far, you've learned the whole flow of designing everything from antennas to PAs, rectifiers, thermal and wireless-power links in one project with Aether, and taking the results out as files. The next part is the index for looking things up.

11 PART

Complete Menu · Ribbon Reference

The 11 menus and 8 ribbon tabs of Aether Desktop 2026 V2.3 were read one by one from the real screen and organized here. Item names are **the English names exactly as they appear on screen**, with the shortcut and what each does. Open this part when you don't know where a feature is.



How to read
A row marked ▶ is a submenu, and the indented rows below it are its items. The same function often appears in the menu, the ribbon and the right-click menu together. How to use the new features is in Chapters 43–50.

11.1 File menu

Item	Shortcut	What it does
New Project	Ctrl+N	Create an empty project.
New from Template...		Open one of 18 starter projects (basics · antennas · RF circuits / PCB · analysis) as an unsaved copy. Each template lists the steps to try.
Open Project...	Ctrl+O	Open a .warp or CAD file. A 3D preview on the right, resizable columns, and type-to-find (Korean initial consonants work too).
Insert Design from File...		Add a design from another .warp to the current project (a number is added if the name clashes).
Save Project	Ctrl+S	Save all designs of the project into one .warp.
Save Project As...	Ctrl+Shift+S	Save under another name.
Close Project	Ctrl+W	Close the project (asks whether to save).
Import S-Parameter → Matching PCB...		Read an S-parameter (Touchstone) file and create a matching-circuit PCB design.
▶ Export		Result-export group.
CAD Geometry...		Save the geometry as a CAD file.
3D Viewer (three.js)...		A standalone HTML viewer that opens in a browser without Aether (Ch. 44).
Solution Data...		Save the solution data to a file.
DXF Drawing...		2D or 3D-surface DXF drawing (mm).
Report...		PDF report with model, settings, S-parameters and convergence.
Paper...		IEEE two-column paper draft (.tex · figures · .bib; .docx · .pdf on request).
Exit		Quit the program.

11.2 Edit menu

Item	Shortcut	What it does
Undo	Ctrl+Z	Undo.
Redo	Ctrl+Y	Redo.
Cut	Ctrl+X	Cut the selected objects.
Copy	Ctrl+C	Copy the selected objects.
Paste	Ctrl+V	Paste.
Paste & Move	Ctrl+Shift+V	Paste and go straight into move mode.
▶ Select		Selection group.
by Area Filter...		Pick objects by area conditions.
All		Select everything.
Same Material		Select every object of the same material.
Connected Copper (Net)		Select electrically connected copper (a net) in one go.
Paste at Offset...		Paste at a given offset distance.
▶ Duplicate		Duplication group.
Along Line...		Duplicate along a line with a count and spacing.
Around Axis...		Rotational sweep around an axis.
Mirror...		Mirror copy.
Sweep Face Along Normal...		Push the selected face along its normal to give thickness.
Move Faces...		Move faces to change dimensions.
Detach Faces (new object)...		Detach faces into a new object.
Move by Two Points...	Ctrl+M	Move by 'from point → to point' (Z kept).
Rotate by Points...		Rotate by clicking points.
▶ Arrange		Move · rotate · mirror · scale group.
Move...		Move by entering values.
Rotate...		Rotate by entering an angle.
Mirror...		Mirror copy.
Scale...		Change the scale.
Measure / Dimensions...	M	Measure distance · angle · circle. Shown as a table; 'Keep on screen' leaves a dimension line in the 3D view.
▶ Measure by clicking		Measure by clicking only.
Distance		Distance between two points.
Angle		Angle of three points.
Circle		Circular sheet.
Resize to Dimensions...		Resize to target dimensions.

Item	Shortcut	What it does
Edit Dimensions / Expressions...		Edit dimensions with expressions and variables.
Warps Import Status...		A table of unresolved items in an imported Warps design.
Design Variables...		Design-variable table (input to optimization · parametric study).
Box Select (Ctrl+drag)		Box-area selection.
Invert Selection	Ctrl+I	Invert the selection.
Isolate Selected		Show only the selected objects.
Show All		Show everything hidden.
Clear Selection	Esc	Clear the selection.
Delete Selected	Del	Delete the selection.
Group Selection	Ctrl+G	Group the selection.
Ungroup	Ctrl+Shift+G	Ungroup.
Click Selects Whole Group (Alt+click: one)		Clicking selects the whole group (Alt+click selects just one).

11.3 View menu

Item	Shortcut	What it does
Fit All	Ctrl+D	Fit everything in view.
Fit Selection	Shift+F / Ctrl+Shift+D	Fit the selection.
Isometric	Alt+click corner	Isometric view.
Top (XY)	Alt+click top	View from above (XY).
Bottom (XY)	Alt+click bottom	View from below.
Front (XZ)		Front (XZ).
Back (XZ)		Back (XZ).
Left (YZ)	Alt+click left	Left (YZ).
Right (YZ)	Alt+click right	Right (YZ).
Alt+click View Snapping...		Settings for snapping the view with Alt+click.
Shaded		Shaded face display.
Shaded + Edges		Shaded with edge lines overlaid.
Wireframe		Wireframe display.
Solid Display		Toggle opaque solid display.
▶ Look		Display-style group (display only; selection · snapping · drawing unchanged). The choice is remembered.
Realistic		Default realistic display.
2D Toon		Webtoon-style flat colors with ink outlines.
Blueprint		Blueprint style.
Pencil Sketch		Pencil sketch with hatching in the shade.

Item	Shortcut	What it does
X-Ray		Glass-like display where every layer · via · sheet is visible at once.
Height Colors		The z height of each body with a color scale and legend.
▶ Lighting		Lighting group.
Camera Headlight		Light that follows the camera (default).
Work Plane		Lighting relative to the work plane.
Fixed (legacy)		Old fixed lighting.
Brighter (+10%)		10 % brighter.
Dimmer (−10%)		10 % dimmer.
Brightness...		Set brightness directly.
Reset		Reset lighting.
Display Diagnostics...		A table that checks the display state (triangle count, hidden objects and so on).
Auto Display on Open		On open, apply hidden region / PML and opaque conductors automatically (when off, shown as saved).
Show Regions / PML		Show the hidden air region and PML.
Toggle Dark Theme		Switch the dark screen theme.
Tooltips on/off		Turn help bubbles on or off.

11.4 Project menu

Item	Shortcut	What it does
▶ Insert		Design-insertion group.
Warps Design		Add an empty Warps (driven) design next to the existing ones.
Warps Eigenmode Design		Add an eigenmode design.
Design from File...		Add a design from another .warp.
Duplicate Design		Duplicate a design (geometry · settings · reports, not the solution).
Rename Design...		Rename the design.
Delete Design...		Delete the design (after confirming; the last one cannot be deleted, use Close Project).
Add Material...		Add a new material.
Edit Materials...		Edit the material table.

11.5 Draw menu

Item	Shortcut	What it does
Box		3D box. Draw with the mouse and Tab to enter values; Shift+click opens a dialog.
Cylinder		Cylinder.
Sphere		Sphere.
Cone		Cone.
Torus		Torus.

Item	Shortcut	What it does
Rectangle		Rectangular sheet.
Circle		Circular sheet.
Ellipse		Elliptical sheet.
Regular Polygon		Regular polygon (+ / - changes the number of sides).
Line		A line or, with a width, a wiring trace.
Polyline		A multi-point line. Click the first point to close into a face.
Helix		Helix.
Repeat Last Draw	Space	Run the previous drawing tool again (Space).
Import CAD...		Import STEP · IGES · DXF and others (materials assigned automatically from layer names).
RF Circuit Wizard...		Synthesize RF patterns from a circuit model (the same family as Filter Designer).
Filter Designer...		Design LPF · HPF · BPF · BSF as patterns · chip RLC · hybrid.
Place Component... (Diode · PA · IC ...)		Place parts such as diodes · PAs · ICs.
▶ Auto Feed Network		Automatic feed-network design group.
Auto Feed Network...		Automatically generate a feed network joining the selected port ends.
Edit...		Edit again the feed network (or Smart Connect) you made.
Verify / Tune...		Verify and tune the feed network with EM.
Bondwire...		Draw an HFSS-style wire bond (JEDEC4/5, Low) from pad point to lead point. It is solved as a real solid.
Transmission Line Wizard...		Transmission-line design wizard (Ch. 19).
Antenna Wizard...		Antenna synthesis wizard for 22 families (Ch. 20).
Antenna Designer...		Antenna designer.
PA Wizard...		Power-amplifier matching · performance wizard (Ch. 23).
Impedance Matching Wizard...		Impedance-matching wizard (Ch. 22).
Bias Network Designer...		Bias-circuit designer.

11.6 Modeler menu

Item	Shortcut	What it does
Relative CS from Picked Point...		A relative coordinate system whose origin is the clicked point.
Relative CS (type origin)...		Create a relative coordinate system by typing the origin.
Working Coordinate System...		Change the working coordinate system.
Boolean...		Boolean (unite · subtract · intersect) dialog.
Unite Selected		Unite the selected objects.
▶ Subtract		Subtract group.
Selected (first – others)		Subtract the others from the one picked first.
Selected, Keep Tools		Subtract while keeping the others (tools).

Item	Shortcut	What it does
Subtract...		Pick target and tools in a dialog and subtract.
Separate Bodies		Separate a united object.
Replace CAD Source...		Swap in a different CAD source file.
Arrange...		Move · rotate · mirror · scale in one dialog.
Duplicate...		Duplication dialog.
Copy & Move by Two Points...		Copy while moving by two points.
Mirror by Two Points...		Mirror-move across the plane defined by two points.
Mirror Copy by Two Points...		Mirror-copy using two points.
Rotate by Points...		Rotate by clicking points.
Split...		Cut an object with a plane.
▶ Sweep		Sweep group.
Around Axis...		Rotational sweep around an axis.
Along Vector...		Sweep along a vector.
Along Path...		Sweep along a path.
Face Along Normal...		Sweep a face along its normal.
Equation Based Curve...		Create a curve from an equation.
Cover Lines		Make a face from closed lines.
Line Pattern...		Repeat a pattern along a line.
Meander...		Meander line. With 'Fix length' off the length can grow or shrink; there is a live preview and length readout.
▶ Smart Connect		Join two line ends with a taper, step and so on.
Smart Connect...		Pick two ends and generate the connection.
Edit...		Edit again the feed network (or Smart Connect) you made.
Tune...		Tune the connection you made.
▶ Auto Feed Network		Automatic feed-network design group.
Auto Feed Network...		Automatically generate a feed network joining the selected port ends.
Edit...		Edit again the feed network (or Smart Connect) you made.
Verify / Tune...		Verify and tune the feed network with EM.
Stub (Radial / Class F)...		Generate a radial (fan) or Class F stub.
▶ RF		RF design-tool group.
Z0 Line (λ/4, MS / CPW / CPWG)...		A line of target Z0 (including λ/4) as microstrip · CPW · CPWG.
C / L from a Line...		Make a C or L from a line stub. Stub shape (rectangle · round · fan · N-gon), synthesis mode, both-side placement and 3D preview.
Filter / Match...		Generate filter · matching structures from lines.
Class F on Output Line...		Generate a Class F harmonic termination on the output line.
SMD Part (R / L / C)...		Place an SMD part. The pad1 → pad2 angle can be set freely.

Item	Shortcut	What it does
Place SMD at Point...		Hover over a point for a 3D preview, click to pin (Enter place, Esc cancel).
Via Fill / Smart Via...		Fill the selected copper area with vias (automatic pitch · rules).
Overlap & Clearance...		Overlap · clearance check.
Design Rule Check (DRC)		Design-rule check.
PCB Helical Coil (through vias)...		A PCB helical coil wound through vias.
Move Faces...		Move faces to change dimensions.
Detach Faces (new object)...		Detach faces into a new object.
Move Edges...		Move edges.
Fillet Edges...		Round edges.
Chamfer Edges...		Chamfer edges.
Delete Selected		Delete the selection.

11.7 Simulation menu

Item	Shortcut	What it does
Via Model for Simulation...		Settings for how vias are modeled in the analysis.
▶ Assign		Assignment group.
Boundary...		Assign a boundary condition (PEC · radiation · finite conductivity · lumped RLC and so on).
Wave Port...		Assign a wave port.
Lumped Port...		Assign a lumped port.
Create Open Region (Radiation / PML)...		Automatically create an air box and radiation boundary or PML from the wavelength at a frequency.
▶ Add		Addition group.
Solution Setup...		Add a solution setup (default order First order).
Frequency Sweep...		Add a frequency sweep (Discrete · Interpolating · Fast).
Mesh Operation...		Specify a local mesh.
Generate Mesh...		Generate the mesh in advance.
Validation Check	F5	Pre-analysis check (F5). A coarse discrete sweep is warned about.
Setup Advisor...		Check solution settings and propose with evidence (Ch. 43).
Analyze All	F9	Run the full analysis (F9).
Thermal Analysis...		Run thermal analysis.

11.8 Results menu

Item	Shortcut	What it does
Create Modal S-Parameter Report		S-parameter report (graphs · tables).

Item	Shortcut	What it does
Compare with Circuit Model...		Overlay the EM result on a stored circuit model (only designs made with Filter Designer · RF synthesis).
Port Modes Table		Port-mode table.
Eigenmode Data		Eigenmode frequency · Q table.
Far Field Radiation Pattern...		Far-field pattern (gain · directivity · realized gain).
Antenna Parameters vs Frequency...		Gain · efficiency · radiation versus frequency.
Expression Plot (Output Variables)...		Plot an output-variable expression.
Output Variables...		Define expression variables from S-parameters and others.
Edit Sources...		Edit excitation amplitude · phase (for beam synthesis and so on).
Field on Line...		Graph of field values along a line.
3D Radiation Pattern		3D radiation pattern. Peak shown, peak-phase button, animation.
Convergence Table		Convergence table per adaptive pass.
▶ Export		Result-export group.
S-parameters...		Save as Touchstone (.sNp), with port-name comments.
Report...		PDF report with model, settings, S-parameters and convergence.
Paper...		IEEE two-column paper draft (.tex · figures · .bib; .docx · .pdf on request).
Export...		Export result data.
▶ PA Results		Power-amplifier result group (Ch. 23). All results are grouped below.
Show Boundaries and Ports		Show boundaries · ports.
Show Radiation Boundary		Show the radiation boundary.
Hide PML Layer		Hide the PML layer.
Hide Grid Plane		Hide the grid plane.
S-Parameter Metrics...		A table of metrics such as bandwidth and minimum S11.
Vector Fit / SPICE Macromodel...		Fit the S matrix with rational functions and download a .subckt macromodel (needs scikit-rf, 8 or more frequency points).
Parameter Study Results...		Parametric-study results.
Plot Field Overlay...		Overlay fields.
E Field |E|		Show the electric field |E| (phase animation).
H Field |H|		Show the magnetic field |H|.
Surface Current |Js|		Show the surface current |Js|.
Field on Cut Plane		Field on a cut plane.
Nonlinear Co-sim (SPICE + EM)...		Couple SPICE diodes and the EM solution by harmonic balance (Ch. 25).
Rectifier Report...		Rectifier summary report (Pin sweep · power budget · BV warning).
Rectifier Plots...		Rectifier efficiency graphs (versus Pin · load R_L · f0).
Circuit + EM (co-sim)...		Joint circuit and EM analysis.

Item	Shortcut	What it does
3-Line De-embedding...		3-line de-embedding.

PA RESULTS SUB-ITEMS

	All PA results...
Summary	Performance summary · Operating points below P1dB · Where the numbers come from
Power sweep	Pout, gain, DE, PAE vs Pin · Gain, DE, PAE vs Pout · AM-AM / AM-PM · Drain current and DC power
Efficiency	Efficiency vs back-off
Frequency	Power vs frequency · Gain and load penalty vs frequency · Power sweeps at the band edges
Linearity	Two-tone: carrier, IM3, IM5, OIP3 · Linearity vs efficiency · Two-tone spectrum
Load and layout	Load-pull contours and presented load · Load-pull points vs model · Layout of the drawn PA
Simulation	Co-simulation S-parameters · Co-simulation stability
PCB analysis	PCB: EM · PCB · PCB: amplifier S11, S22, gain · PCB: Psat · PCB: Smith chart · PCB
Thermal	Heat vs input power · Junction temperature vs input power · Pout under the Tj limit · Tj vs ambient · Operating point vs cooling · Heat path

11.9 WPT Beam menu

Item	Shortcut	What it does
Link Budget vs Distance...		Link budget versus distance (Ch. 26).
Beamforming / Focusing...		Beam steering · focusing.
Distance Sweep...		Distance sweep.
Rectenna / RX...		Rectenna receiver model.
Field Slice / 3-D Beam...		Field slice and 3D beam.
FEM Check...		Verify with FEM.
Cavity WPT Designer...		Automatic cavity-resonator WPT design (Ch. 46).
▶ Example:		Nine built-in examples (cavity 433 MHz · 2.4 GHz, RX offset, R_L, exposure, tracking, spiral · SRR resonators, TM010 cavity).
RX Position / Attitude...		RX position · attitude (tilt · rotation · polarization) loss.
Rectifier Load R_L...		PCE · Vdc versus load resistance.
Exposure Map...		Power-density map and recommended transmit power.
Tracking Demo...		Moving-RX tracking (line · circle · figure-8).
Open Example (8×8 focus demo)		Open the 8×8 focus example.
Guide...		WPT usage guide.
Resonator WPT Designer...		Planar-resonator CMT link design.
Cavity Resonator Designer...		Cavity-resonator (rectangular · cylindrical) design.

11.10 Tools menu

Item	Shortcut	What it does
RF Power & Trace Check...		Check RF power and trace width · allowable current.

Item	Shortcut	What it does
BOM Export (CSV)...		Parts list as CSV.
BOM Export grouped by value (CSV)		BOM grouped by value.
Design Variables...		Design-variable table (input to optimization · parametric study).
Solver and Mesh Controls...		Detailed solver · mesh settings.
Engineering Diagnostics...		Analysis-diagnostics table.
Parameter Study...		Sweep variables and solve repeatedly.
Parameter Study Results...		Parametric-study results.
Optimization...		Optimization (Nelder-Mead · Pattern · L-BFGS-B · Differential evolution · Bayesian/TPE (needs optuna)). Define design variables and bind them to basis-order exponents first.
RF Wizard Tune Results...		RF-wizard tuning results.
Optimization Results...		Optimization results.
Stop Analysis (keep results)	Shift+Esc	Stop the analysis and keep results so far (Shift+Esc).
Abort Analysis (immediately)		Abort the analysis immediately.
Keyboard Shortcuts...		Shortcut list.
Scripting Console		Scripting console (Python).
Clear Messages		Clear the message window.
Nonlinear Co-sim (SPICE + EM)...		Couple SPICE diodes and the EM solution by harmonic balance (Ch. 25).
Device Library...		Diode-model library (HSMS · SMS · NT series, datasheet sources cited).
PA Library...		PA chip library of 17 types.
Circuit + EM (co-sim)...		Joint circuit and EM analysis.

11.11 Help menu

Item	Shortcut	What it does
About Aether Desktop		Version information.

11.12 Buttons by ribbon tab

Ribbon buttons are one-click versions of the menu items above. The buttons gathered in each tab are as follows.

Home

New · Open · Save · Close · Template · Box · Cylinder · Sphere · RF Wizard · Transmission Line Wizard · Antenna Wizard · Antenna Designer · PA Wizard · Impedance Matching Wizard · Bias Network Designer · Boundary · Open Region · Port (pick) · Wave Port · Setup · Sweep · Validate · Analyze · Thermal · Stop · Abort · Report · Export · Export Report · PA Results

Draw

Box | Cylinder | Sphere | Cone | Torus | Rectangle | Circle | Ellipse | Polygon | Bondwire | Line | Polyline | Helix | Import | Repair Bodies | S-Param PCB | RF Wizard | Smart Connect | Filter Designer | Auto Feed Network | Feed Tune | Transmission Line Wizard | Antenna Wizard | Antenna Designer | PA Wizard | Impedance Matching Wizard | Bias Network Designer

Modeler

Work Plane | Coordinate System | Undo | Redo | Copy | Cut | Paste | Paste & Move | Smart Connect | Boolean | Unite | Subtract | Separate | Split | Slice | Move by points | Rotate by points | Arrange | Copy & Move | Mirror | Mirror Copy | Along Line | Around Axis | Mirror... | Around Axis | Along Vector | Along Path | Equation Curve | Helix | PCB Helix | Spiral | Cover Lines | Line Pattern | Meander | Stub | Z0 Line | C / L | Filter / Match | Class F | SMD Part | SMD @ Point | Via Fill | Clearance | DRC | Feed Network | Measure | Resize | Parameters | Variables | Export CAD | Sweep Face | Move Faces | Detach Faces | Move Edges | Fillet | Chamfer | Add Material | Edit Materials | Delete | »

Simulation

Diagnostics | Controls | Air Region | Optimize | Parameter Study | Study Results | Stop | Abort | Assign | Open Region | Lumped RLC | Lumped Port (pick) | Wave Port (pick) | Wave Port... | Lumped Port... | Add Setup | Add Sweep | Mesh Operation | Generate Mesh | Validate | Analyze All | Stop | Abort | Thermal

Thermal

Thermal Settings | Thermal Materials | Transistor | Heat Source | RF Loss → Heat | Face BC | Contact / TIM | Thin Copper | Via Wizard | Copper Coin | Heat Spreader | PCM | Pulse / Duty | Run Thermal | Force re-solve | Stop | Temperature Map | Heat Path | Compare / Sweep | Optimize Tj | Temp → RF | Export Field CSV | Thermal Guide

Results

S-Parameters | Port Modes | Eigenmodes | Radiation | Antenna | Expression | Field on Line | Convergence | E / H Field | Surface Current | Cut Plane | 3D Pattern | Mesh View | Export | Metrics | Export Report

WPT Beam

Link vs distance | Distance sweep | Beamforming | Field slice | Rectenna | FEM check | Cavity 433 MHz | Cavity 2.4 GHz | Cavity FEM | Exposure map | Tracking demo | RX pose | Load R_L | Example | Guide | Resonator WPT | Cavity

View

Fit All | Fit Selection | Iso | Top | Front | Right | Shaded | Edges | Wireframe | Solid | Looks | Why blank?



Now it's your turn to bring your imagination to life as real circuits and antennas!

Draw your first drawing boldly with the wizards, doubt your ports meticulously, confirm convergence with the adaptive mesh, and close the last link of a perfect design with cool, runaway-free cooling and bench measurements.

WARPSOLUTION Inc.

www.warpsolution.com

Aether EM Practical Design Guide (Desktop 2026 V2.3) · Created by Kyung-hak Lee · together with the six friends

Aether · Porty · Wavy · Mesh · Wiz · Thermy